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Electrical Characterization and Modeling of Gate-Last Vertical InAs Nanowire MOSFETs on Si

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Abstract—Vertical InAs nanowire transistors are fabricated on Si using a gate-last method, allowing for lithography-based control of the vertical gate length. The best devices combine good on- and off-performance, exhibiting a on-current of 0.14 mA/µm, and a sub-threshold swing of 90 mV/dec at 190 nm L_G. The device with the highest transconductance shows a peak value of 1.6 mS/µm. From RF measurements, the border trap densities are calculated and compared between devices fabricated using the gate-last and gate-first approaches, demonstrating no significant difference in trap densities. The results thus confirm the usefulness of implementing digital etching in thinning down the channel dimensions.

Index Terms—Vertical, nanowire, InAs, MOSFET, transistor, gate-last, self-aligned.

I. INTRODUCTION

In recent decades, the fast development of integrated circuits has been based on the scaling of planar Si metal-oxide-semiconductor field-effect transistors (MOSFETs). Extremely scaled devices often suffer from various short channel effects (SCEs), leading to larger power dissipation and lower operational frequencies. In order to reduce SCEs, new gate architectures and materials are implemented to improve the electrostatic control of the MOSFET channel and the carrier transport properties, respectively [1]–[4]. Vertical III-V compound semiconductor nanowire transistors are an attractive option due to integration compatibility of high electron mobility III-V materials on Si and straightforward fabrication of gate-all-around structures [5]–[7]. Furthermore, the vertical geometry allows for large contact regions and gate length optimization without affecting the device footprint.

The performance of vertical nanowire MOSFETs is commonly restricted by high access resistances situated in the ungated regions. These resistances can be lowered by highly doped access regions, strain engineering or through the use of heterostructures to reduce the metal-semiconductor contact resistance. However, in order to achieve a minimal resistive contribution of the access regions, a gate overlapping the contacts is needed. In this letter, vertical InAs nanowire MOSFETs fabricated using a self-aligned, gate-last process [8] are presented exhibiting excellent on- and off-state performance. The devices are studied by both DC and RF-characterization to evaluate the limiting contributions of the transistor design and the quality of the gate stack. A comparison is made between these gate-last fabricated devices and gate-first devices to evaluate the high-k oxide quality to their respective channels.

II. DEVICE FABRICATION

The schematic layer structure of the nanowire MOSFETs is shown in Fig. 1a). The devices are fabricated on lowly p-doped Si {111} substrates with a 300-nm-thick epitaxially grown InAs layer [9]. InAs nanowires are grown in two types of arrays with nanowire-center-to-center spacings of 200 nm and 500 nm, respectively, using metalorganic vapor phase epitaxy (MOVPE) where Au particles are used as seeds. The growth itself is a two-step process resulting in a 200-nm-long unintentionally doped InAs bottom part and a 400-nm-long highly Sn-doped top section. During the latter section, a highly doped shell around the unintentionally doped bottom segment is also formed. The final nanowires have a length of about 600 nm, a core diameter of 35 nm and a shell thickness of about 10 nm. The carrier concentration of the unintentionally doped segment and the highly doped part of the nanowires is estimated from to be on the order of $1 \times 16 \text{ cm}^{-3}$ and $1 \times 19 \text{ cm}^{-3}$, respectively from back-gated field-effect measurements on similar nanowires. To define the gate length ($L_G$), hydrogen silsesquioxane (HSQ) is spin-coated followed by electron-beam exposure and development, where the exposure dose determines the HSQ thickness [10]. Three different gate lengths between 70 and 200 nm are utilized. The W/TiN top metal stack is defined using anisotropic dry etching, followed by HF etching of the HSQ layer. A 10-nm-thick SiO$_2$ is defined to serve as a first spacer layer. In this step, only the channel region is unprotected, as the bottom part is covered by SiO$_2$ and the top part by the top metal. The channel region is digitally etched by oxidizing the InAs surface in O$_3$, followed by HCl : H$_2$O (1:10) etching to remove the formed oxide. The digital etching is repeated until the highly doped shell is removed and the desired nanowire

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larger access resistances in the top of the nanowires than in the bottom. This device data is fitted to the virtual source model [14] with an injection velocity \( \nu_{\text{inj}} \) of \( 2.1 \times 10^7 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1} \) and a mobility of \( 1200\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1} \) for the bottom grounded data. Here, a semiconductor capacitance (0.4 aF/\( \mu \text{m} \)) normalized to \( L_G \) in strong accumulation is assumed and calibrated to measured capacitance values from [15] for similar InAs nanowire diameters and gate stack. The same model can be used for the top grounded case with the exception of reversed access resistances and a lowered \( \nu_{\text{inj}} \), which is attributed to a small potential barrier close to the top of the nanowires, possibly originating from the W/InAs junction. Evidently, the used gate-last process results in an asymmetric transistor structure, and consequently quantities like the access resistance and \( \nu_{\text{inj}} \) will differ in the two bias directions. The drain-induced barrier lowering (DIBL) is found to be \( 70\text{ mV V}^{-1} \) and \( 56\text{ mV V}^{-1} \) at \( I_D = 1\mu \text{A} \mu \text{m}^{-1} \) in the bottom grounded and top grounded biasing directions, respectively. The difference in DIBL between the two cases correlates to lower output conductance when keeping the top grounded. The difference is, however, mostly attributed to different \( \nu_{\text{inj}} \), with a smaller electric field along the channel needed to saturate the carrier velocity for lower \( \nu_{\text{inj}} \). The DC-performance is mostly limited by high source/drain access resistance, indicated by the on-resistance \( (R_{\text{on}}) \) of \( 1300\Omega \mu \text{m} \).

For each of the three \( L_G \), the two 200-nm-spaced devices with the highest \( g_m \) is subjected to virtual source modeling. The \( \nu_{\text{inj}} \) scaling trend shown in Fig. 1d) corresponds well to previously reported values for InAs HFETs [16]. Also, the measured \( R_{\text{on}} \) (extracted at \( V_{DS} = 0 \text{V} \) and \( V_{GS} = 0.7\text{ V} \)) for the same devices are shown to follow a linear trend. From the \( R_{\text{on}} \) corresponding to an \( L_G \) of 0, the total access resistance \( (R_S + R_D) \) is found to be about \( 650\Omega \mu \text{m} \). By comparing the resulting \( g_m \) when keeping the bottom of the nanowires as ground to measurements when grounding the top, it is established that most of this access resistance is situated close to the top of the nanowires. This is supported by the virtual source modeling of the devices in Fig. 1d), which yields a mean \( R_D/R_S \) of 1.8. The dimensions for the devices in Fig. 1d) are provided in the figure caption.

The MOSFETs with a nanowire spacing of 500 nm exhibit much lower \( R_{\text{on}} \) as compared to the 200-nm-spaced devices, as seen in Fig. 1d). No clear trend with respect to \( L_G \) is observed in the data, probably due to a higher sensitivity to process variations as the resistance is lower. The lower resistance for these devices results in much improved \( g_m \), as shown in Fig. 2a) where a \( g_{m,\text{max}} \) of \( 1.6\text{ mS} \mu \text{m}^{-1} \) is obtained for the best device. A possible explanation for the lower on-resistance for these devices is partly attributed to a higher doping-level in the overgrown shell, originating from changed materials competition between nanowires for different spacings. The higher doping level allows for lower resistance in the semiconductor and lower metal-semiconductor contact resistance. The sub-threshold characteristics, however, are severely degraded such that \( I_D \) is only modulated by one order of magnitude over the full \( -0.4\text{ V} \leq V_{GS} \leq 0.7\text{ V} \) voltage swing. The changed characteristics could be attributed to the top metal edge being positioned lower and closer to the foot of the
nanowires, originating from the spin-on technique. The bottom of the nanowires has a thicker shell and, for these transistors, is insufficiently etched during the digital shell etching.

IV. RF CHARACTERIZATION

To validate the transistor geometry and to analyze the quality of the high-κ oxide in the gate-last fabricated transistors in comparison to a gate-first process, a 200-nm-spaced transistor is characterized at radio frequencies by vector network analyzer measurements. The $g_m$ and output characteristics for this transistor are shown in Fig. 2. After off-chip calibration and on-chip de-embedding of the measurement pads, the unilateral power gain ($U$), the current gain ($h_{21}$), the maximum stable gain (MSG), the maximum available gain (MAG), and the stability factor ($K$) are calculated and presented as a function of frequency in Fig. 3a). The maximum oscillation frequency ($f_{\text{max}}$) and transition frequency ($f_T$) are found to be 48 GHz and 25 GHz, respectively. In order to determine the limiting factors of the high-frequency performance, the parameters of the small-signal model [17] shown in Fig. 3b) are extracted. The frequency-dependent $g_{\text{GD}}, g_{\text{GS}},$ and $g_m$ are included to simulate the trap response of the high-κ oxide assuming a uniform trap distribution. The small-signal $g_m$ corresponding to DC (27 mS) correlates well with the intrinsic $g_m$ obtained by virtual source modeling, 26.9 mS (1.11 mS μm$^{-1}$). Further agreement between the models can be seen in the access resistances, which for the virtual source model correspond to 14.3 Ω (347 Ω μm) and 11.8 Ω (286 Ω μm) for $R_D$ and $R_S$, respectively. The real border trap densities ($N_{\text{bt}}$) in the gate oxide are extracted from the RF data according to [18], Fig. 4. A comparison of the data in this letter with the trap response of gate-first fabricated InAs nanowire MOSFETs [19] indicates that the gate-last process has very similar trap densities as compared to the gate-first fabricated device. Furthermore, low-frequency (10 Hz – 1 kHz) noise measurements (not shown) indicates comparable border trap densities deeper in the oxide for the two processing schemes. The RF performance is mainly limited by the large parasitic gate-source capacitance ($C_{\text{GS}}$), originating from a large overlap area between the gate electrode and the 

InAs epitaxial layer (72 μm$^2$) and a too thin bottom spacer layer (10 nm), which is confirmed by cross-sectional SEM. $C_{\text{GS}}$ together with the other capacitances given in the small-signal model is also responsible for the decrease in Re$(\gamma_{21})$ at high frequencies shown in Fig. 4a). This decrease is not inherent to $g_m$ itself and thus prevents probing the border trap density closer to the channel interface.

V. CONCLUSION

In this work, vertical nanowire MOSFETs fabricated using a self-aligned gate-last process are realized. Using this process, a good combination of on- and off characteristics for vertical III-V nanowire MOSFETs is achieved with $SS = 90 \text{mV/decade}$ and $I_{\text{on}} = 0.14 \text{mA μm}^{-1}$. The trimming of the channel dimension using digital etching is found to have no significant impact on the gate stack quality.

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