Vertical InAs nanowire MOSFETs with $IDS = 1.34 \text{ mA/\mu m}$ and $gm = 1.19 \text{ mS/\mu m}$ at $VDS = 0.5 \text{ V}$

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Vertical InAs Nanowire MOSFETs with $I_{DS} = 1.34$ mA/μm and $g_m = 1.19$ mS/μm at $V_{DS} = 0.5$ V

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III-V MOSFETs are currently considered for extension of, or as an add-on to, the Si CMOS technology. Following the Si-technology evolution, it is attractive to consider advanced III-V transistor architectures with non-planar geometry and improved electrostatic control [1]. We report on vertical InAs single nanowire FETs with diameter of 45 nm diameter, integrated on Si substrates with $L_G = 200$ nm. The devices demonstrate normalized extrinsic $g_m$ and $I_{DS}$ of 1.34 S/mm and 1.19 A/mm, respectively, at a $V_{DS}$ of 0.5 V, and with an on-resistance of 321 Ωμm, all values normalized to the circumference. The improvements in $g_m$ and $I_{DS}$ as related to previous work [2] are attributed to the improved high-κ interface consisting of Al₂O₃/HfO₂, as well as to the nanowire source resistance, which is reduced by applying an inorganic spacer layer. The main performance limitation is identified as the drain resistance in the ungated top part of the wire. By scaling the NW diameter to 28 nm, we also observe subthreshold swing down to 80 mV/decade at 50 mV $V_G$. Performance is still limited by parasitic contact pad capacitances, originating from the limitations of the optical lithography used.

A 4” highly resistive Si wafer, which is overgrown with a 300-nm-thick InAs buffer layer, serves as sample substrates [3]. Electron-beam-lithography defined gold particles placed in arrays prior to epitaxial growth are made on 2x2 cm² pieces. Each sample has 160 FETs, both single- and multi-wire devices, with RF compatible layout. High-k gate oxides are deposited with an ALD process consisting of 0.5 nm Al₂O₃ at 250 °C and 6.5 nm HfO₂ at 100 °C, directly after epitaxial nanowire growth. For device isolation and stray capacitance minimization, source mesas are etched out from the buffer layer. In a novel fabrication procedure, the first spacer layer, separating source and gate, is formed by plasma-enhanced-chemical-vapor-deposition of 60 nm Si₃N₄. The sputtered tungsten gate is defined using an etch mask and a dry-etch procedure. The top spacer layer separating gate and drain is made of a spin-coated organic film and has a thickness of 150-250 nm, making the ungated top part of the wire the largest fraction of the series resistance that limit the performance.

DC characterization is performed for single and multi NW InAs NW FETs, where the best single NW device of 45 nm diameter shows a normalized $I_{DS}$ of 1.82 mA/μm and 1.34 mA/μm at a $V_{GS}$ of 1.0 V and $I_{DS}$ of 0.5 V, respectively. These devices also show a corresponding $g_m$ of 1.45 mS/μm and 1.19 mS/μm at a $V_{DS}$ of 1.0 V and 0.5 V, respectively. The $V_t$ is extrapolated using the maximum transconductance method and determined to -0.27 at $V_{GS} = 0.5$ V. The device shows a low hysteresis of less than 5 mV at a $V_{DS}$ of 0.5 V, most likely due to a low trap concentration within the low temperature deposited HfO₂ film. Devices scaled in diameter to 28 nm, with a 5.0-nm-thick Al₂O₃/HfO₂ film, and with 96 wires in parallel show a normalized $I_{DS}$ of 0.112 mA/μm, a transconductance of 0.154 mS/μm, and a $V_t$ of -0.23 V at a $V_{GS}$ of 0.5 V and within 0.5 V $V_{GS}$. While the performance is lower in the on-state, the subthreshold swing is greatly improved down to 80 mV/decade at a $V_{GS}$ of 50 mV. Data for both samples is benchmarked in Table 1 [4], demonstrating good performance as compared to alternative implementations. S-parameter measurements of our RF devices with 45 nm in diameter, show that FETs consisting of 192 wires in parallel, operate with $f_i = 18.5$ GHz and $f_{max} = 32.2$ GHz. Although these values represent a two fold increase to previous published data for InAs NW FETs [5], the performance is still limited by parasitic contact pad capacitances, originating from the limitations of the optical lithography used.

Fig 1. SEM images (30° tilt angle) of a single NW (a) and an array of NWs (b) after ALD as well as a 192 NW array with etched-out source mesa and sputtered W-gate-pad (c).

Fig 2. Schematic cross-section showing the different layer thicknesses in the fabricated device.

Fig 3. SEM image (30° tilt angle) of a single NW after the gate length definition.

Fig 4. Normalized $I_{DS}$ vs $V_{DS}$ for a single 45 nm NW FET. Fig 5. Normalized $g_m$ vs $V_{GS}$ for a single 45 nm NW FET.

Fig 6. Normalized $I_{DS}$ vs $V_{GS}$ for a single 45 nm NW FET. Fig 7. Normalized $I_{DS}$ vs $V_G$ for a 28 nm NW array FET.

Fig 8. Normalized $I_{DS}$ vs $V_{DS}$ for a 28 nm NW array FET. Fig 9. Normalized $g_m$ vs $V_{GS}$ for a 28 nm NW array FET.

Table 1. Data benchmark for this work and other high performance technologies at a $V_{DS}$ of 0.5 V and a $V_{OD}$ of 0.5 V