High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors

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Abstract—We present electrical characterization of GaSb/InAs(Sb) nanowire tunnel field-effect transistors. The broken band alignment of the GaSb/InAs(Sb) heterostructure is exploited to allow for inter-band tunneling without a barrier, leading to high on-current levels. We report a maximum drive current of 310 \( \mu \text{A/\mu m} \) at \( V_{DS} = 0.5 \text{ V} \). Devices with scaled gate oxides display transconductances up to \( g_m = 250 \text{ mS/mm} \) at \( V_{DS} = 300 \text{ mV} \), normalized to the nanowire circumference at the axial heterointerface.

Index Terms—Tunnel field-effect transistors (TFET), broken gap, InAs, GaSb, III-V

I. INTRODUCTION

The rapid development of semiconductor technology during the last few decades has resulted in high-performance transistors in both Si and III-V semiconductor technologies [1], [2]. However, MOSFETs suffer from a fundamental lower limit of 60 mV/decade subthreshold swing (SS) at room temperature, and a corresponding lower limit of the power dissipation at a given threshold voltage and on-current level. There is a demand for devices with very steep inverse transconductance, with a p+−n+ junction.

A major advantage of such devices, such as tunnel field-effect transistors (TFETs), lies in the possibility of reducing the series resistance, allowing for a one-step fabrication process for the source and drain electrodes. In order to minimize potential leakage current in the channel, and to reduce the cross-sectional area of the conducting channel, the nanowires were annealed in \( H_2 \) during the final stage of the growth, forming a constriction at the axial GaSb/InAs(Sb) heterointerface [9]. As a reference, nanowires were also grown where the Zn-doping and \( H_2 \) annealing were omitted. Assuming a hole mobility between 70 cm\(^2\)/Vs (calculated from [12]) and 700 cm\(^2\)/Vs [1], and a measured resistivity of 7.1 m\( \Omega \cdot \text{cm} \) [9], we estimate the carrier concentration in the GaSb segment to be in the range 1.3 \( \cdot 10^{18} \) - 1.3 \( \cdot 10^{19} \) cm\(^{-3}\). A corresponding estimate for the InAs(Sb) segments yields a carrier concentration of 6 \( \cdot 10^{17} \) cm\(^{-3}\) [13].

After the growth, the nanowires were dry-deposited onto prepatterned Si chips with a 100-nm-thick thermally grown SiO\(_2\). Source and drain electrodes were defined by electron beam lithography (EBL) followed by thermal evaporation of Ni and Au. A lift-off window for the high-\( \kappa \) dielectric was defined by EBL, followed by an atomic layer deposition of an Al\(_2\)O\(_3\)/HfO\(_2\) bi-layer (2/70 cycles) both deposited at 100 \( ^\circ \text{C} \) corresponding to an EOT of 2 nm, assuming \( \epsilon_r = 15 \). As a final step, a Ni/Au top-gate was formed. All room temperature
measurements were carried out in darkness and vacuum.

III. RESULTS AND DISCUSSION

Fig. 2 presents the output characteristic for a reference device without a constriction at the axial heterointerface (as displayed in the schematics in Fig. 1b) and without Zn doping in the GaSb segment. In this device, carrier transport can occur along the InAs(Sb) shell and across the GaSb/InAs(Sb) heterojunction simultaneously due to the ambipliability of the core-shell system [12]. At negative gate bias, the InAs(Sb) is depleted of electrons and the majority of the current is forced through the heterojunction. At positive gate bias, electrons accumulate at the surface, enabling n-type conduction along the shell with reduced tunneling. It is not possible to turn this device off.

Fig. 2 displays the output characteristic for a device with a Zn-doped GaSb segment and where a constriction has been formed at the axial heterointerface (d = 35 nm ± 5 nm). We calculate an on-current of 91 µA/µm ± 13 µA/µm at V_DS = VGS - VT = 0.5 V (normalized to the nanowire circumference, π · d), and a maximum on-current of 310 µA/µm ± 45 µA/µm (V_DS = 0.5 V, VGS - VT = 2 V), corresponding to R_ON = 1.57 Ω · mm, exceeding the drive currents of e.g. stacked AlGaSb-InAs TFETs [6].

As illustrated, the device in Fig. 2 has a 35 nm gate underlap to the heterojunction. In an ideal case, this would constitute a tunnel junction integrated in series with an InAs(Sb) MOSFET. Such a tunnel junction is normally open for conduction due to the broken gap, and the current is modulated by the gate-action imposed on the InAs(Sb) segment. In the off-state, the device will suffer from the ungated segment, allowing tunneling across the heterostructure. Minority carriers (holes) injected from the drain may also accumulate and become trapped under the gate due to a barrier in the valence band to the GaSb.

The output characteristics of a device where the gate overlaps the heterojunction is included in Fig. 2c & d. The better off-state device performance we attribute to two effects: (i) the improved electrostatics at the heterojunction, gating the constriction rather than the thicker InAs(Sb), in agreement with the results of Tomioka et al. [5] and (ii) the device design layout itself as discussed next. For the device in Fig. 2c & d, where the gate overlaps the heterointerface, we argue that in the on-state, the bands in the GaSb and the InAs(Sb) bend downwards. The bands are likely more easily modulated in the InAs(Sb) segment but some modulation of the GaSb is also expected. This may compromise the on-state by forming a barrier in the valence band in the GaSb segment, and reduce the probability of inter-band tunneling. However, Fermi level movement in GaSb-based MOS-structures is typically difficult due to the high number of acceptor-like interface traps (Dit) between GaSb and high-κ dielectrics [14]. In addition, the high Zn-doping level of the GaSb should lead to a limited movement of the bands on the GaSb side. For this reason, we argue that a device with a gate overlap better cuts off the tunneling path at the source heterojunction, which is otherwise open for an underlapping device (Fig. 2b). Furthermore, the improved electrostatics at the constriction may lead to a better gate response. However, the devices are sensitive to measurement history, charging and hysteresis effects which makes the analysis somewhat challenging, e.g. determining a well-defined threshold voltage. The devices presented above show the extremes of a number of devices studied.

Evaluating the negative differential resistance region in the underlapping device, we calculate a maximum peak-to-valley current ratio of 3 with a maximum peak-current of 240 kA/cm² (forward biased with the InAs(Sb) segment grounded). We observe that V_P remains constant, or moves to slightly higher V_DS bias with increasing gate bias. In the ideal case of a gated resistance (MOSFET) integrated in series with a passive tunnel junction we expect V_P to move to lower V_DS values with increasing gate bias. The lack thereof indicates that the band alignment at the tunnel junction is affected by the gate.

Fig. 3 displays the transfer characteristic of a device where the EOT is scaled to 1.3 nm and the gate has been aligned to the heterointerface (~5 nm overlap), with L_G = 290 nm. We calculate an on-current of 62 µA/µm at V_DS = 0.3 V and VGS - VT = 0.5 V, V_T = -0.51 V, and a maximum on-current of 130 µA/µm (V_DS = 0.3 V, VGS - VT = 1.75 V). The drain-induced barrier lowering was determined between V_DS = 0.05 and 0.3 V to be 280 mV/V. The maximum I_ON/I_OFF ratio increases from 143 at RT to 10^4 at 4.2 K and the SS decreases with temperature from 320 mV/decade at 295 K
to 17 mV/decade at 4.2 K as seen in the inset of Fig. 3a. Similar values have been reported in other III-V TFET devices [15]. The temperature dependent $SS$ is likely a result of trap-assisted tunneling via the high $D_{it}$ at the high-$\kappa$/semiconductor interface. The determined activation energy, when reverse-biased, in the off-state from Fig. 3a (not shown) corresponds to the band gap of InAs$_{0.9}$Sb$_{0.1}$ (0.27 eV). Furthermore, the onset of a temperature-independent ambipolar current is also evident in Fig. 3a & b, most likely due to band-to-band tunneling at the gate-drain junction related to the narrow band gap of the InAs(Sb). The temperature dependence of the valley current (forward-biased with InAs(Sb) grounded, not shown) suggests activation energies well-below $E_F/2$ of InAs(Sb) indicating that trap-assisted tunneling is limiting the off-state performance.

Fig. 3: Electrical data for a nanowire TFET, $d = 45$ nm, where the gate oxide thickness is scaled to 5 cycles of Al$_2$O$_3$ and 50 cycles of HfO$_2$. The data is normalized to the constriction circumference. (a) Temperature dependent $I_{DS}$-$V_{GS}$ characteristics at $V_{DS} = 50$ mV from 4.2 K up to 295 K in increments of approximately 50 K. The inset shows the subthreshold swing as a function of temperature. (b) Temperature dependent $I_{DS}$-$V_{GS}$ characteristics and (c) transconductance at $V_{DS} = 300$ mV from 4.2 K to 242 K. $\Delta T \approx 50$ K.

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