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High-Frequency InGaAs Tri-gate MOSFETs with $f_{\text{max}}$ of 400 GHz

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind

We report on extremely scaled down tri-gate RF MOSFETs utilizing lateral nanowires as the channel, with gate length and nanowire width both of 20 nm. These devices exhibit simultaneous extrapolated $f_i$ and $f_{\text{max}}$ of 275 and 400 GHz at $V_{\text{GS}} = 0.5$ V, which is the largest combined $f_i$ and $f_{\text{max}}$, as well as the largest $f_{\text{max}}$ reported for all III-V MOSFET.

Introduction: Tri-gate (or non-planar) MOSFETs for RF-applications are motivated by that the use of a high-k oxide, rather than a semiconductor barrier (as in HEMTs) allows for higher gate capacitance in the MOSFET [1-2]. Furthermore, the tri-gate architecture improves short-channel effects, allowing for shorter gate length, $L_g$, without degradation of performance due to short-channel effects. Both these points enable higher ideal transconductance, $g_{\text{m}}$, in MOSFETs compared to HEMTs, assuming similar electron mobility. In fact, state-of-the-art III-V MOSFET devices exhibit $g_{\text{m}}$ larger than that of record HEMTs, although they presently do not allow RF-compatible device designs [3-5].

In this work, we present RF-compatible tri-gate In$_{0.53}$Ga$_{0.47}$As MOSFETs utilizing lateral nanowires (NWs) as the channel. Compared to our previous work, we have here further scaled down device dimensions, $L_g$ and nanowire width, $W_{\text{NW}}$ [6]. This enables higher $g_{\text{m}}$ at $V_{\text{GS}} = 0.5$ V, which significantly improves $f_i$/$f_{\text{max}}$ from 220/305 GHz to 275/400 GHz. The combined $f_i$ and $f_{\text{max}}$, as well as the $f_{\text{max}}$ of these devices represent the highest reported values for all III-V MOSFETs.

Results: Fig. 2a shows transfer characteristics of a device with $L_g = 20$ nm measured at DC with a Keithley 4200 semiconductor characterization system. All data is normalized to the total gated periphery of the NWs (7 µm). At $V_{\text{DS}} = 0.5$ V, peak $g_{\text{m}}$ is 2.1 mS/µm. Fig. 2b shows the scaling behaviour of peak $g_{\text{m}}$ and on-resistance $R_{\text{on}}$, versus $L_g$. $R_{\text{on}}$ reaches 220 Ωm at $L_g = 20$ nm. The total access resistance is estimated to 130 Ωm from transmission line measurements.

RF-measurements were performed at 40 MHz to 67 GHz with an Agilent E8361A vector network analyser. On-chip pad de-embedding as well as off-chip two-port load-reflect-reflect-match calibration was performed. The total pad capacitances were approximately 20 fF.

A small-signal model was determined from the measured S-parameters, with a good fit to the measurement data [8]. Fig. 3 shows measured and modelled (dashed traces) unilateral power gain $|S_21|$ and maximum available/stable gain (MSG) and [MSG] for a device with $L_g = 20$ nm. Extrapolated cut-off frequency $f_i$ is 275 GHz and maximum oscillation frequency $f_{\text{max}}$ is 400 GHz.

The small-signal model, which is similar to that in [6], includes both the effect of border traps in the oxide, and impact ionization. Border traps are modelled using the distributed border trap model in [9]. Border traps introduce a frequency-dependency to $g_{\text{m}}$ and $g_{\text{ds}}$, as well as a frequency-dependent oxide loss, and explain the -10 dB slope of $|S_11|$ versus $f$ [10]. Fig. 4a shows $g_{\text{mes}}$ for an $L_g = 20$ nm device extracted from the small-signal model at DC and 67 GHz (RF). $g_{\text{mes}}$ increases by approximately 13% in the latter case, to a maximum of 2.9 mS/µm at $V_{\text{DS}} = 1.25$ V, which is attributable to that trap responses are partially disabled at high frequency.

The effective gate resistance is ~5 Ω, and the source and drain resistances is ~2 Ω. The gate-to-source and gate-to-drain capacitances, $C_{\text{GS}}$ and $C_{\text{GD}}$, are shown in Fig. 4b. At $V_{\text{DS}} = 0.5$ V, the total gate capacitance $C_{\text{GS}} + C_{\text{GD}}$ is 15 F at peak $g_{\text{m}}$. This includes both the parasitic capacitance from the source and drain gate overlaps, and the intrinsic gate capacitance. The latter is estimated as $C_{\text{G}} = (2/3)W(L/W)C_{\text{ox}}$, with the quantum capacitance $C_{\text{q}} = \sqrt{q^2m^*}h^2$, which is ~2 fF with $m^* = 0.04m_0$. Thus, RF-performance is primarily limited by the parasitic overlap capacitance, which can be lowered by implementation of source and drain spacers.
Fig. 4 Peak $g_m$ and capacitances

(a) Peak $g_m$ measured at both 40 MHz (DC) and 67 GHz (RF), for an $L_g = 20$ nm device.

(b) Gate-to-source, $C_{GS}$, and gate-to-drain, $C_{GD}$, capacitances measured at different $V_{DS}$.

Fig. 5 shows a benchmark of $f_t, f_{max}$ and the geometric mean $\sqrt{f_t \times f_{max}}$ (dashed traces) for state-of-the-art III-V MOSFETs [11-18]. The geometric mean is 330 GHz for these devices, which is the highest reported value for a III-V MOSFET. Squares show planar devices, and triangles show non-planar devices.

**Fig. 5 Benchmark of RF-performance for III-V MOSFETs**

Squares show planar devices, triangles show non-planar devices. $V_{DS}$ and $L_g$ varies between devices, but is 0.5 V and 20 nm, respectively, for this work. Dashed traces show the geometric mean.

**Conclusion:** We have demonstrated $L_g = 20$ nm In$_{0.53}$Ga$_{0.47}$As tri-gate MOSFETs with record high-frequency performance, $f_t = 275$ GHz and $f_{max} = 400$ GHz at $V_{DS} = 0.5$ V.

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