Nanostructures for Optoelectronics
Device Fabrication and Characterization
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2018

Link to publication

Citation for published version (APA):
Hultin, O. (2018). Nanostructures for Optoelectronics: Device Fabrication and Characterization. Division of Solid State Physics, Department of Physics, Lund University, Box 118, SE-221 00 Lund, Sweden.

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Nanostructures for Optoelectronics
Device Fabrication and Characterization

OLOF HULTIN
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Abstract

The nanoscale is an exciting domain when it comes to crystal growth, light-matter interaction and electronics. Especially for optoelectronics, semiconductor nanostructures have many advantages compared to traditional planar structures and are highly interesting for the next generation of solar cells, photodetectors and light emitting diodes. This dissertation explores device fabrication, and electrical and electro-optical characterization of semiconductor nanostructures, with an emphasis on materials and structures suitable for optoelectronics.

The first part gives an overview of nanowire synthesis, doping and current challenges in the field.

The second part describes doping characterization at the nanoscale using electrical measurement techniques. A fabrication scheme for creating nanowire devices for Hall effect characterization and field-effect characterization is presented. Methods for simulating electric transport in nanowires to analyze measurements and determine doping concentration from Hall and field-effect measurements are discussed. Doping incorporation in InP core-shell nanowires is studied with Hall effect and correlated to optical characterization techniques. An experimental comparison between nanowire Hall effect measurements and field-effect measurements is presented. A three-probe device geometry to simplify Hall effect measurements is suggested and experimentally verified. Hall measurements are performed on nanowire-based platelet-structures.

The last part of the dissertation describes fabrication and characterization of nanoscale optoelectronic devices. Nanowires with p-n junctions synthesized using the high-throughput and substrate-less Aerotaxy method are characterized and shown to have promising properties. Finally, fabrication and electro-optical characterization of nitride platelet LEDs with emission from UV to red is presented.

Key words Nanowire, Characterization, Hall effect, Solar cell, Light-emitting diode (LED)
Nanostructures for Optoelectronics

Device Fabrication and Characterization

Olof Hultin

Doctoral dissertation
2018

Lund University

Department of Physics
Division of Solid State Physics
Front cover: Scanning electron micrograph showing an array of AlGaN platelet UV LEDs. The oxide passivation has been etched away from the top of the structures to allow electrical contact only to the p-side. © Olof Hultin.

Back cover: Colorized scanning electron micrograph of an InP nanowire device for Hall effect and field-effect characterization. © Olof Hultin.

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Printed in Sweden by Media-Tryck, Lund University
Lund 2018
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Abstract

The nanoscale is an exciting domain when it comes to crystal growth, light-matter interaction and electronics. Especially for optoelectronics, semiconductor nanostructures have many advantages compared to traditional planar structures and are highly interesting for the next generation of solar cells, photodetectors and light emitting diodes. This dissertation explores device fabrication, and electrical and electro-optical characterization of semiconductor nanostructures, with an emphasis on materials and structures suitable for optoelectronics.

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List of papers

This dissertation is based on the following papers, which will be referred to in the text by their Roman numerals. The papers are appended at the end of the dissertation.

I. **Synthesis of doped InP core-shell nanowires evaluated using Hall effect measurements**  
M. Heurlin, O. Hultin, K. Storm, D. Lindgren, M.T. Borgström, L. Samuelson  
Nano Letters 14 (2), 749-753 (2014)  
I performed the device processing, electrical measurements, simulations, analysis of the electrical data, and wrote part of the paper.

II. **Study of carrier concentration in single InP nanowires by luminescence and Hall measurements**  
D. Lindgren, O. Hultin, M. Heurlin, K. Storm, M.T. Borgström, L. Samuelson, A. Gustafsson  
Nanotechnology 26 (4), 045705 (2015)  
I performed the device processing, electrical measurements, simulations, and analysis of the electrical data.

III. **Comparing Hall Effect and Field Effect Measurements on the Same Single Nanowire**  
O. Hultin, G. Ottes, M.T. Borgström, M. Björk, L. Samuelson, K. Storm  
Nano Letters 16 (1), 205-211 (2016)  
I designed the experiment and the devices, performed the device processing, electrical measurements, simulations, data analysis and wrote the main part of the paper.
IV. **Simplifying nanowire Hall effect measurements using a three-probe device geometry**  
*O. Hultin*, G. Otnes, M.T. Borgström, M. Björk, L. Samuelson, K. Storm  
Nano Letters 17 (2), 1121-1126 (2017)  

I designed the experiment and the devices, performed the device processing, electrical measurements, simulations, data analysis and wrote the main part of the paper.

V. **GaAs nanowire pn-junctions produced by low-cost and high-throughput Aerotaxy**  
*These authors contributed equally  

I designed the devices, performed the device processing, electrical measurements, analysis of the electrical data, and wrote a large part of the paper.

VI. **Dislocation-free Designed Sub-micron Nitride Platelets for UV to Red LEDs**  
*O. Hultin*, A. Nowzari, L. Wendt, M. Khalilian, Z. Bi, T. Lu, B.J. Ohlsson, B. Monemar, A. Gustafsson, K. Storm, L. Samuelson  
In preparation 2018  

I designed most of the devices, performed most of the device processing, electrical measurements, analysis of the electrical data, and wrote the main part of part of the paper.
The following papers are not included in the dissertation, but show related work I have contributed to:

VII. **Doping evaluation of InP nanowires for tandem junction solar cells**
F. Lindelöw, M. Heurlin, G. Otnes, V. Dagytė, D. Lindgren, **O. Hultin**, K. Storm, L. Samuelson, M.T. Borgström
Nanotechnology 27 (6), 065706 (2016)

VIII. **InP nanowire p-type doping via Zinc indiffusion**
T. Haggren, G. Otnes, R. Mourão, V. Dagyte, **O. Hultin**, F. Lindelöw, M.T. Borgström, L. Samuelson

IX. **High In-content InGaN nano-pyramids: Tuning crystal homogeneity by optimized nucleation of GaN seeds**
Z. Bi, A. Gustafsson, F. Lenrick, D. Lindgren, **O. Hultin**, L.R. Wallenberg, B.J. Ohlsson, B. Monemar, and L. Samuelson

X. **Electrical and optical evaluation of n-type doping in In\textsubscript{x}Ga\textsubscript{1-x}P nanowires**
X. Zeng,*, R. T. Mourão,*, G. Otnes,*, **O. Hultin**, V. Dagytė, M. Heurlin, M. T. Borgström
*These authors contributed equally
Nanotechnology 2018

XI. **Hall Effect Measurements in Nanowires.**
**O. Hultin**, K. Storm, and L. Samuelson
Invited chapter in 21st century handbook of nanoscience
Taylor and Francis Books
In preparation 2018
Populärvetenskaplig sammanfattning

På nanoskalan fungerar fysiken inte riktigt som vi är vana vid i makro-världen. I strukturer som har ungefär samma storlek som våglängden för synligt ljus (400-700 nm) uppstår flera intressanta fenomen som kan utnyttjas för att bygga mer effektiva optoelektroniska komponenter, exempelvis lysdioder (LED) och solceller. Lysdioder används idag i belysning och förbättringar i effektivitet kan ge mycket stora energibesparingar globalt. Solceller är nu i många lägen ett kostnadseffektivt alternativ till fossilbränslen för elproduktion och marknaden står därmed inför en förväntad explosionsartad tillväxt. Teknik som förbättrar effektiviteten kan få stort genomslag och är mycket viktigt både för pris och resursutnyttjande.

Att bygga komponenter på nanoskalan medför dock en hel del utmaningar. Den här avhandlingen behandlar hur man kan mäta elektriska materialegenskaper i nanostrukturer, hur man kan utföra mätningar på solceller på nanoskalan, samt hur man kan bygga lysdioder av nanostrukturer.

Nanostrukturer som studeras i avhandlingen är baserade på halvledande nanotrådar. Nanotrådar är trådformade halvledarkristaller som ofta har en diameter kring 100 nm (ca en tusendel av ett hårstrås diameter) och en längd på några mikrometer. Avhandlingen behandlar främst material lämpade för användning i lysdioder (GaN) och solceller (InP, GaAs). På grund av nanotrådarnas stora yt/volymförhållande och små dimensioner har de en förmåga att hantera de mekaniska spänningar som uppstår när man kombinerar material med olika gitteravstånd i samma kristall. Detta gör att det går att växa nanotrådar med tidigare omöjliga materialkombinationer i mycket hög materialkvalitet, vilket är avgörande för goda optiska och elektriska egenskaper. En annan egenskap som gör nanotrådar intressanta är att de kan fungera som vågledare för ljus, vilket gör att ljus kan absorberas från en yta som är betydligt större än nanotrådens tvärsnittsarea. I en solcell kan därför nanotrådar placeras med ett visst mellanrum i en periodisk matris och ändå absorbera i princip allt inkommande ljus. Detta möjliggör en materialbesparing på mellan 5 och 10 gånger.

Den första delen av forskningen som beskrivs i avhandlingen rör mätning av laddningsbärarkoncentration (elektroner eller hål) i nanostrukturer. Laddningsbärarkoncentrationen i en halvledare kontrolleras vanligen genom tillförsel av främmande ämnen, dopatomer. Noggrann kontroll över laddningsbärarkoncentration och dopingkonzentration är mycket viktigt då det påverkar materialets konduktivitet, elektriska potentialstruktur, laddningarnas livstid,


Sammanfattningsvis, avhandlingen utforskar karakteriseringsmetoder för halvledande nanostrukturer, i synnerhet strukturer och material som är intressanta för nästa generations elektrooptiska komponenter, exempelvis solceller och lysdioder. Metoderna är generaliserabara även för andra typer av nanostrukturer lämpade för exempelvis transistorer och högspänningslektronik.
1. Introduction

The world is currently facing one of the greatest challenges in modern times, the transition from reliance on fossil fuels to an ecologically sustainable energy system. This transition involves both switching to energy production based on renewable sources and reducing energy consumption by using energy more efficiently.

As of 2015, about 23% of the global electricity was produced from renewable sources. Solar photovoltaic electricity production has had a remarkable growth of more than 6000% between 2005 and 2015, but still accounts for only 1% of the total electricity production. The growth potential is huge, since the total influx of energy from the sun is about four orders of magnitude larger than the total electricity production today. The photovoltaic market is dominated by crystalline silicon solar cells and the average efficiency of solar panels being installed today is around 17%. The quick increase in installed capacity is driven largely by a rapid decrease in semiconductor module cost. The module cost is now only around 30% of the total cost of a utility-scale photovoltaic installation. As the semiconductor module cost becomes a smaller part of the total cost, reducing the price of the module will have less and less effect on the total cost. By instead increasing the power conversion efficiency of the module, the power production density increases and all costs that scale with area are reduced. This allows further cost reduction, motivating research on a new generation of high-efficiency photovoltaics. While silicon solar cells have seen a slow increase in efficiency in recent years, III-V multi-junction solar cells have reached efficiencies close to 50%. These cells, based on elements in group III and V of the periodic table, are however prohibitively expensive due to high material cost and a costly production process.

Lighting is a significant part of the total global energy consumption, accounting for 15% of the electricity produced in the United States during 2015. A transition to efficient light emitting diode (LED) based lighting is projected to decrease the energy consumption for lighting in the U.S. by 75% in the year 2035. What we perceive as white light is really a combination of red, green and blue light. Most white LED lamps today are based on a blue GaN light emitter and a lossy down-conversion by phosphors to emit longer wavelengths. A more efficient way to generate white light is to have color-mixing LEDs directly emitting in blue, green and red. However, while blue LEDs have very high efficiency, green LEDs have poor efficiency and high-efficiency red LEDs are made in another material system (AlGaInP), making them more complicated to integrate in a color-mixing lamp. Increasing the efficiency of nitride based LEDs in
green and red is a hot research topic, not only for lighting applications but also for efficient direct-view displays. Current and projected long-term efficacies for the major competing LED lighting technologies are presented in table 1.1. The efficacy of color-mixing LED is currently low primarily due to the poor efficiency of green LEDs.

### Table 1.1. LED efficacy projected by U.S. DOE.5

<table>
<thead>
<tr>
<th>Technology</th>
<th>2016 status</th>
<th>Long-term goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phosphor-converted LED (cool white)</td>
<td>160 lm/W</td>
<td>255 lm/W</td>
</tr>
<tr>
<td>Color-mixing LED</td>
<td>&lt;100 lm/W</td>
<td>325 lm/W</td>
</tr>
<tr>
<td>OLED</td>
<td>60 lm/W</td>
<td>190 lm/W</td>
</tr>
</tbody>
</table>

Many of the challenges optoelectronics are facing can be addressed by the use of engineered nanowire-based nanostructures. Nanowires are high aspect ratio structures with a diameter in the nanometer scale and much larger length, typically a few micrometers. Since the size is close to the wavelength of visible light, nanowires have interesting light-matter interaction properties that make them especially interesting for optoelectronic applications.

Nanowires can be made either by top-down or bottom-up processes. A top-down process typically consists of etching out nanowires from a bulk material using lithography techniques to control the structure. This method is similar to the methods used in the semiconductor industry to produce high-quality silicon structures. Silicon is however rather unique concerning how well it etches and produces passivating native oxide. Other materials, such as III-V semiconductors are more challenging to etch with as good structural control and without compromising the material quality. In the bottom-up approach, nanostructures are formed directly by crystallization of growth precursors in gas or liquid form. This self-assembling of atoms can be utilized to synthesize monocrystalline, high quality nanostructures with uniform size distribution.6–8

The first study of self-assembled nanowire-like structures was presented already in 1964, when Wagner & Ellis at Bell labs grew silicon “whiskers” from gold catalysts and described the vapor-liquid-solid growth mechanism. Wagner & Ellis realized the potential of the method and stated already from the beginning that it can be used to synthesize dislocation-free crystals from different materials, p-n junctions and even hetero junctions.9

It was not until the 1990s that nanowire research really took off. Nanowires were grown from different III-V materials10–12 and more advanced structures such as atomically sharp hetero junctions were realized.13–16 In the years following, it was shown that nanowires could be functionalized and put to use in actual devices. Nanowire transistors7,17–20, LEDs18,21–24, solar cells25–29, tunnel diodes,7,30 and TFETs31–34 were presented.

Today, many academic research groups and companies are developing nanowire devices for both basic research and commercial applications. Nanowires have many very
advantageous properties that will be discussed in the coming chapters. For nanowire devices to compete with established technologies, extremely good control of structural, optical and electrical properties is necessary. This necessitates accurate and reliable characterization methods.

1.2 Scope

The topic of this dissertation is device fabrication and characterization of electrical and optical properties of III-V and III-nitride nanostructures. The main themes are doping characterization using Hall effect and field-effect measurements (papers I-IV), and fabrication and characterization of nanoscale optoelectronic devices (papers V-VI).

In chapter 2, synthesis and doping of nanowire-based structures is discussed. An overview of previous work in doping characterization at the nanoscale is given.

Chapter 3 discusses fundamental properties of solar cells and LEDs and reviews previous work in nanoscale semiconductor optoelectronics.

In chapter 4, methods for doping characterization at the nanoscale are discussed in more detail, device fabrication is described, theoretical models used in the papers are derived, and the work presented in papers I-IV is discussed.

Chapter 5 discusses the optoelectronic characterization done in papers V-VI: an investigation of the properties of nanowires fabricated using the high-throughput and substrate-less Aerotaxy method, and fabrication and characterization of nanowire-based nitride platelet LEDs emitting from UV to red.

The last chapter contains concluding remarks and an outlook.
2. Nanowire synthesis

There are many different ways to synthesize nanowires. The nanowires in this dissertation have been synthesized by metal-organic vapor phase epitaxy (MOVPE), where the growth precursors are supplied in the vapor phase, typically as metal-organic molecules such as trimethylindium (InC$_3$H$_9$). When exposed to the high temperature of the growth reactor, the metal-organic molecules decompose and the group III and group V atoms are released to be incorporated in the growing crystal. Nanowire growth can be catalyzed by a metallic seed particle in vapor-liquid-solid (VLS) growth as first described by Wagner & Ellis$^9$, or grown on a substrate covered by an inert growth mask where crystals only can nucleate in the openings of the mask (selective area growth). A more recent invention is the Aerotaxy process, where nanowires are grown from a seed particle in the aerosol phase, without the need of a growth substrate.$^{35}$ Finally, we discuss growth of more complex platelet-structures. For a more in-depth discussion, there are several extensive reviews on the subject.$^{8,36-39}$
2.1 Vapor-liquid-solid growth

A metal seed particle deposited on a crystalline substrate is the starting point for nanowire synthesis with the VLS method. The seed particles can be generated in a particle generator and deposited in random patterns or be deposited in ordered arrays using lithographic techniques.\(^8\) The basic steps of the VLS method are:

- **Annealing the substrate and seed particles in the growth reactor.** This removes oxides and other contaminants and may make the seed particles form a liquid alloy with the substrate. (Figure 2.1a).

- **Introduction of growth precursors to initiate the growth.** Due to the high temperature, the growth precursors crack into their constituents and may diffuse on the substrate. Typically, group III elements are incorporated in the seed particle and when the concentration reaches a critical level (super-saturation), solid crystalline material (the nanowire) nucleates at the liquid-solid interface. (Figure 2.1b). How the group V elements reach the growth interface is not yet fully understood. One possibility is that they travel along the growth interface.\(^8\)

- **Nanowire growth.** Under the right conditions, the seed particle is located on top of the growing nanowire and the precipitation of material makes the nanowire grow layer by layer in a step-flow process. The growth can be terminated by stopping the flow of precursors when the desired length is reached. (Figure 2.1c and 2.1d).

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**Figure 2.1.** Growth of nanowires via the vapor-liquid-solid method. a) Annealing in the growth chamber b) Introduction of growth precursors to initiate the growth. c) When the seed particle is super saturated, a nanowire starts to grow by precipitation at the liquid-solid interface. d) The growth is terminated by stopping the flow of group III precursors when the desired length is reached.
Radial growth on the nanowire side facets or substrate surface (directly from gas phase to solid phase) may compete with the growth catalyzed by the seed particle. To minimize this, VLS synthesis is usually carried out at relatively low temperatures, 350-550°C. The growth rate is typically on the order of nanometers per second. VLS is the most common and well-studied mechanism for nanowire growth.

2.2 Selective area growth

In selective area epitaxy, the crystalline growth substrate is covered by an inert mask, typically made out of SiNₓ or SiOₓ. By using lithography and etching, nano-sized openings are made in the mask. Under the right conditions, growth is inhibited on the mask and nanowires only nucleate in the mask openings. The growth can be controlled so that the nanowire grows predominantly in the axial direction. The selectivity comes from differences in atomic incorporation rate on the different facets. With this method, the nanowire size and array geometry can be controlled with great precision. The basic steps of substrate patterning and selective area epitaxy are:

- Deposition of a growth mask, e.g. by low-pressure chemical vapor deposition. (figure 2.2a)
- Spin-coating the substrate with an electron-sensitive resist (figure 2.2b).
- Defining holes in the resist in a lithography process and etching away the exposed growth mask in a dry etch process (figure 2.2.c)
- Removing the remaining resist using solvents to prepare the substrate for growth (figure 2.2.d)
- Nucleation and growth of nanowires under supply of growth precursors (figure 2.2e-2.2f)
Figure 2.2. Patterning of growth mask and nanowire synthesis by selective area epitaxy. a) A growth mask is deposited on the substrate. b) A layer of resist is spin-coated on the sample. c) Resist patterned by electron beam lithography. The pattern is transferred to the growth mask by dry etching. d) Resist removed. e) The semiconductor crystals nucleate only in the mask openings. f) Nanowire growth under precursor flow. g) The growth is terminated by stopping the flow of growth precursors when the desired length is reached.

The growth substrates used for the selective area epitaxy in this dissertation were patterned with electron beam lithography. Alternative lithography techniques include nanoimprint lithography, interference lithography and Talbot lithography. The lack of a seed particle is advantageous since foreign material may have detrimental effects on the semiconductor. Most notably, gold forms a deep level trap in Si, making integration of Au seeded VLS nanowires on Si problematic. Selective area epitaxy also simplifies synthesis of core-shell structures since there is no catalyst to interfere with the radial growth. Selective area epitaxy is usually conducted at slightly higher temperature than VLS, 500-750°C for most III-V materials. The growth rates are comparable.
2.3 Aerotaxy growth

In VLS and selective area nanowire synthesis, a significant part of the material and cost is the crystalline substrate. Aerotaxy is a synthesis technique where nanowires are grown from a seed particle in the aerosol phase without the need of a substrate. The method was first presented by a group from Lund in 2012.35 The basic steps of Aerotaxy are:

- Generation of aerosol seed particles e.g. using an arc reactor (figure 2.3a)
- Compaction of seed particles in a tube furnace (figure 2.3b)
- Size selection of the seed particles using a differential mobility analyzer. (figure 2.3c)
- Alloying the seed particle with trimethylgallium (TMGa). (figure 2.3d)
- Growth of nanowires under supply of growth precursors (figure 2.3e)
- Collection of nanowires on a substrate (figure 2.3f).

![Figure 2.3. Growth of nanowires by Aerotaxy. a) Generation of aerosol seed particles. b) Compaction of seed particles. c) Size-selection of seed particles. d) Alloying the seed particle. e) Nanowire growth. f) Collection of nanowires. Adapted with permission from Springer Customer Service Centre GmbH, Nature 35 copyright 2012.]

Since seed-particles and growth precursors are continuously supplied and the length of the nanowires can be controlled by the growth conditions and chamber length, the method allows continuous production of nanowires. The nanowire growth rate in an Aerotaxy system can be 1µm/s, three orders of magnitude faster than typical substrate based methods. The high growth rate and continuous production makes the Aerotaxy method suitable for large-scale production of nanowires. In paper V, we show that it is possible to use Aerotaxy for production of nanowires with a p-n junction, an important step towards mass-production of nanowire solar cells.
2.4 Axial and radial growth

The discussion above primarily focuses on growth in the axial direction. However, material may also attach to the side facets of the nanowires during the synthesis, making them grow also in the radial direction. This can give the nanowires a radially grown shell and under certain conditions a tapered shape. An unintentional shell can short-circuit axially defined components, but shell growth can be reduced by tuning growth conditions or by in-situ etching.45

Radial growth can also be used to give a nanowire functionality and form a core-shell structure. By using growth conditions that promote radial growth, the nanowire core can be used as a substrate for vapor-solid layer growth of a shell. The function of the shell can for example be to passivate the core15 or to form a radial p-n junction (paper I and II).

One of the most important differences between radial and axial nanowire junctions is the area. A radial p-n junction can have a significantly larger active area than an axial, which is beneficial to decrease the current density in a light-emitting diode. However, a large area p-n junction may lead to more recombination in the depletion region, which lowers the open-circuit voltage in a solar cell.46 For nanowire LEDs, radial p-n junctions are often preferred,47 while the highest nanowire solar cell efficiencies have been achieved with axial junctions.40
2.5 Growth of nitride platelets

Nanowires can also be used as a starting point to form nanostructures that are even more complex. Platelets are III-N structures that can be used as relaxed, dislocation-free c-plane growth templates. To synthesize these structures, pyramid-shaped structures nucleated from nanowire seeds are grown with selective area epitaxy on a patterned substrate with a Si$_3$N$_4$ growth mask. (figure 2.4a and 2.4b). Next, the pyramids are subjected to conditions in the growth reactor where the net incorporation of Ga into the crystal is essentially zero (temperature above the lower limit of GaN sublimation, a NH$_3$ flow, but no Ga flow). Under these conditions, Ga atoms dissociate from the crystal, leading to a surface-bound layer of Ga that can diffuse on the surface and reincorporate in the crystal (figure 2.4c). This causes a net flow of atoms, minimizing the surface energy and creating a flat c-plane that can be used for growth of active layers, e.g. dislocation-free LEDs or electronic devices. The final shape is determined by the relation between the surface energies of the different facets. Since crystal facets with low surface energy typically have higher growth rates, they will disappear during growth and the crystal shape will be dominated by the facets with lower growth rate. The reformation process is therefore necessary to recreate the low-energy surfaces, i.e. the c-plane. Similar approaches can be applied to form both InGaN and GaN platelets (paper VI).

Figure 2.4. Synthesis of sub-micron platelets. a) Nucleation. b) Growth of pyramids. c) Reformation of the pyramids, creating platelets with smooth top facet c-planes.
2.6 Doping

The conductivity of a semiconductor is determined by the charge carrier concentration and the carrier mobility. To control the charge carrier concentration and add functionality to a device, the semiconductor is doped with atomic impurities containing more or fewer valence electrons, thereby adding free electrons or holes to the material. In most planar semiconductors, doping is very well controlled and optimized. Often the doping is done after growth (ex situ), by diffusion or ion implantation.

When adding atomic impurities with more (less) valence electrons than the atoms they replace, donor (acceptor) energy levels are formed close to the conduction (valence) band. These donor (acceptor) states represent loosely bound electrons (holes) that are easily excited to the conduction (valence) band by the thermal energy at room temperature. When electrons (holes) are the majority carriers, the semiconductor is said to be n-type (p-type) and the Fermi level is close to the conduction (valence) band (Figure 2.5).
For n-type doping of MOVPE synthesized III-V materials, it is common to use dopants that replace the group V atom, i.e. group VI elements such as sulfur (S) or tin (Sn). For p-type doping it is common to use group II elements that replace the group III atom, e.g. Zn. Due to the small size and vertical orientation of nanowire devices, ex situ doping is often hard to implement with sufficient accuracy. Instead, doping is commonly introduced during growth (in situ) by supplying doping precursors in the growth chamber. In situ doping is in many ways a more complex topic with many unresolved questions. Some aspects are highlighted below. For a more in-depth discussion, see the reviews by Wallentin and Borgström and Dayeh et al.

In VLS growth, the dopants may incorporate either axially via the seed-particle or through the sidewalls. Incorporation through the sidewalls may give rise to gradients in the doping concentration of the nanowire. There is also evidence that the doping incorporation is not necessarily homogeneous along the interface to the catalyst due to faceting of the growth interface at the VLS junction. In addition, the different diffusion lengths of the growth precursors may give rise to axial doping gradients and due to a reservoir effect from dopants stored in the seed particle, it may be hard to achieve abrupt doping gradients.

Adding doping precursors to the gas mixture may also have effects other than introducing impurities to the semiconductor crystals, e.g. affect the crystal structure. In paper I we show that Sn can affect the growth rate and crystal structure of InP.

It is important to remember that the charge carrier concentration is not always equal to the concentration of dopants. For a dopant to contribute a charge carrier, it must be ionized. The ionization energy is controlled by the properties of the elements and the atomic bonds, e.g. the dopant’s position in the lattice. Usually dopants can be chosen so that they form shallow energy levels and are fully ionized at room temperature. However in some cases, such as for GaN, no shallow acceptors are available and the most commonly used p-dopant, Mg, forms an acceptor level approximately 170 meV from the valence band, giving an ionization rate of less than 1% at room temperature. The activation energy may also be affected by dopants forming complexes or dopants incorporated in lattice sites other than the one intended. These effects may give rise to saturation effects, limiting the maximum achievable charge carrier concentration. The band structure and carrier concentration can also be strongly affected by the surface properties, especially in thin nanowires with large surface to volume ratio. Charge caught in surface traps can increase or decrease the carrier concentration and in some cases even cause full depletion.
2.7 Measuring doping in nanowires

Accurate control of the doping is essential for high-performance semiconductor devices. The doping level influences not only the conductivity, but also many other important parameters such as the band structure, carrier lifetime, depletion widths and current distribution. Measuring the doping in nanostructures introduces a number of new challenges compared to traditional bulk materials. The small dimensions make it necessary to use advanced fabrication processes and careful methodology. The subject has been explored by many researchers and many different methods have been suggested.\(^{48,49}\) The first measurements of mobility and carrier concentration in nanowires were made by the Lieber group in the year 2000.\(^ {55}\) They fabricated back-gated nanowire transistors and extracted the mobility from the transconductance of the devices. Since then, this type of relatively simple field-effect mobility measurement has been perhaps the most common doping characterization method for nanowires. The main drawbacks of the field-effect method is that it relies on a calculated gate capacitance\(^ {56,57}\), can be affected by surface states, is sensitive to contact resistance\(^ {58}\), and only measures the properties close to the surface of the nanowire.

Doping characterization has also been done with capacitance-voltage (CV) measurements both on arrays\(^ {59}\) or single nanowires\(^ {60,61}\). Although this method is very powerful, capacitance measurements on single nanowires require extremely sensitive measurement methods capable of sub-femtofarad resolution.

Hall effect characterization, which for a long time has been one of the most common methods for doping characterization of planar semiconductors, was carried out on nanowires for the first time in 2012.\(^ {62,63}\) Since then, a number of studies employing Hall effect measurements on nanowires have been published.\(^ {64-69}\) (papers I-IV, X) The main benefits of Hall effect characterization is that it measures the carrier concentration over the entire electrically active cross-section of the nanowire, allows measurements with spatial resolution along the nanowire and is less sensitive to critical input parameters such as the gate capacitance. Devices for field-effect and Hall effect characterization are illustrated in figure 2.6.

![Figure 2.6](image-url) Devices for nanowire characterization. a) Back-gated nanowire field-effect transistor. b) Nanowire device for Hall effect measurements.
Other electrical methods to measure doping include thermoelectric measurements\textsuperscript{70,71} and photocurrent\textsuperscript{72–74}. There are also numerous contact-less methods to measure carrier concentration, including photoluminescence (PL)\textsuperscript{75} (paper II), cathodoluminescence (CL) (paper II), Raman\textsuperscript{76}, THz spectroscopy\textsuperscript{77}, secondary ion mass spectroscopy (SIMS)\textsuperscript{78} and atom probe tomography\textsuperscript{50}.

The discussion on doping characterization in this dissertation will focus on Hall effect characterization and field-effect characterization.
3. Optoelectronics

There are a number of properties that make nanowire-based structures especially attractive for use in optoelectronics, and it is likely that optoelectronics is the first application where nanowire-based devices will be used commercially.

First, due to the small footprint and freedom to expand in the lateral dimension, strain induced by growth of layers with different lattice constants or thermal expansion coefficients can be accommodated and be completely removed after just a few hundred nm in nanowires. This unique property makes it possible to grow structures with material combinations that would not be possible in thin-films without creating large amounts of defects. An example is growth of III-V nanowires on silicon substrates for integration with silicon electronics or simply to bring down substrate costs. It also opens up new possibilities for novel material combinations for high-performance multi-junction solar cells and more freedom in choosing materials to tune the emission wavelength in LEDs.

Second, nanowires can be used to grow completely dislocation-free nitride material. Most dislocations from the growth substrate are filtered out and terminated at the top of the substrate due to the small footprint of the nanowires. Dislocations that make it into the nanowire or are created at the interface are however quickly forced out to the surface of the nanowire, making minimal impact on the structure.

Third, in nanowire growth, new growth conditions, crystal structures and growth facets are available. This includes for instance the non-polar m-plane in GaN, which is interesting in order to eliminate the piezo-electric polarization effects in LEDs, growth conditions to bridge the miscibility gap of InGaN, and controlling the crystal structure with the growth conditions.

Last, since nanowires have dimensions comparable to the wavelength of visible light, they couple light in leaky optical modes. This coupling together with resonance effects that appear in periodic arrays makes it possible for nanowires to absorb light from a larger area than their physical cross-section, meaning that an array of nanowires can be made to absorb significantly more light than a thin-film made from the same amount of material. Current top-performing nanowire solar cells decrease the material usage in the active layer compared to thin film solar cells by almost an order of magnitude, reducing cost and environmental impact. The resonant absorption properties depend on the nanowire diameter, length, array symmetry and distance between the nanowires. By tuning these properties it is not only possible to optimize...
the light absorption in a solar cell, but also to engineer photodetectors for specific wavelengths.86

Nanowires have many benefits compared to planar structures. However, no nanowire-based optoelectronic devices are currently on the market and there are still a number of challenges to overcome. Many III-V materials desirable to use in optoelectronic applications suffer from surface defects, causing Fermi level pinning and high surface recombination velocities. The surface properties must be well controlled to achieve high efficiency devices, especially since the surface to volume ratio of nanowires is so large. Another challenge, and the topic of this dissertation, is device processing and characterization of the electrical properties of these nano-sized devices.

3.1 Solar cells

A solar cell is a device that converts the energy of sunlight into electricity. To achieve this, three steps are necessary: generation of an electron-hole pair from absorption of light, separation of the electron and hole (usually by a p-n or p-i-n junction), and extraction of the electron and hole to an electric circuit. The output power is the product of the current and the voltage, i.e. the amount of charge leaving the solar cell and potential difference between the respective carrier distributions. The basic principles of a p-n junction solar cell can be understood from a band diagram and the diode equation.

![Figure 3.1. Sketched band diagram of a p-n junction solar cell.](image-url)

An incident photon with energy larger than the band gap energy can be absorbed in the semiconductor, exciting an electron-hole pair (figure 3.1). The electron-hole pair will initially have an energy corresponding to the photon energy, but since the excited carriers interact strongly with lattice phonons, they quickly relax down to the band
edge, releasing energy to the lattice. The electron and hole can then drift over the p-n junction and diffuse to the contacts (or drift to the contacts in a long p-i-n junction). The carriers can also recombine, radiatively (emitting a photon) or non-radiatively. In non-radiative recombination, the energy in the electron-hole pair is lost to heat. In contrast, the photon emitted in a radiative recombination event can be reabsorbed by the solar cell and still contribute to the output power.

Solar cells are often characterized by the maximum current and voltage they can produce, i.e. the short-circuit current $I_{SC}$ and the open-circuit voltage $V_{OC}$. The current-voltage characteristic of a solar cell can be described by a slightly modified diode equation:

$$ I = I_0 \left( e^{\frac{eV}{nkT}} - 1 \right) - I_{sc} \quad \text{(eq. 3.1)} $$

where $I_0$ is the dark-current, $e$ is the elementary charge, $V$ is the applied voltage, $n$ is the ideality factor, $k$ is Boltzmann’s constant and $T$ is the temperature. When the anode and cathode is short-circuited, current can flow freely: $V = 0$ and $I = I_{sc}$. When the anode and cathode is open, $I = 0$ and the voltage over the p-n junction increases as to cancel the flow of photocurrent, $V = V_{oc}$. When the exponential in equation 3.1 is significantly larger than 1, we get

$$ V_{oc} \approx \frac{n k T}{e} \ln \left( \frac{I_{sc}}{I_0} \right) \quad \text{(eq. 3.2)} $$

The efficiency of a single junction p-n junction solar cell is fundamentally limited by a number of intrinsic loss processes. The dominating ones are the thermalization losses of high-energy electrons and the loss of photons with lower energy than the band gap. The band gap should thus be small enough to allow absorption of most of the sunlight, producing many electron-hole pairs and thus a large current, but large enough to give a large output voltage and not to lose too much energy to thermalization. Shockley and Queisser calculated that the optimum in this trade-off is a band gap slightly larger than 1 eV for illumination from a black-body radiator similar to the sun.

To further understand the loss processes in a solar cell we need to consider some thermodynamics and look briefly at the principles of the energy-balance model. A more thorough description can be found in ref. 90. A solar cell with a finite temperature is a blackbody radiator. If we assume no other losses (i.e. no non-radiative recombination), the incoming light energy must be extracted either as a current or as black-body emission. At open-circuit conditions, no current is extracted and the emission is equal to the absorption. The carriers excited by the incoming sunlight give rise to a separation in quasi-Fermi levels of electrons and holes, i.e. a forward voltage over the p-n junction. When the p-n junction is forward biased, carriers are injected over the junction, and the radiative recombination increases exponentially.

The output current is equal to the difference between the current density generated by the sunlight ($J_{SC}$) and the loss due to recombination ($J_{rec}(V)$):
\[ J = J_{SC} - J_{rec}(V) = J_{SC} - eF_{e0}(e^{\frac{eV}{kT}} - 1), \quad \text{(eq. 3.3)} \]

where \( F_{e0} \) is the black-body radiation at 0V (proportional to the dark-current \( J_0 \)). This gives us the open-circuit voltage in the radiative recombination limit

\[ V_{OC}^{\text{rad}} \approx \frac{kT}{e} \ln \left( \frac{J_{SC}}{eF_{e0}} \right) \quad \text{(eq. 3.4)}. \]

This is very similar to eq. 3.2. We can relate the carrier generation from the sun to the short-circuit current and the dark-current to the blackbody emission when the diode is not illuminated. The blackbody emission (and thus dark-current) can be reduced by only allowing absorption and emission in certain angles. Ideally, a solar cell should only exchange radiation in the solid angle of the sun. In an ordinary planar solar cell, the absorption angle is the solid angle of the sun and the emission angle is the full sphere around the solar cell. This can be thought of as an entropy loss for the light. However, in a concentrator solar cell, the emission angle is decreased and thus the maximum \( V_{oc} \) is increased. The same effect can be attained in designed nanowire structures, where light may be coupled along the length of the nanowires, thus providing asymmetric absorption and emission angles.\(^{90-93}\) By decreasing the entropy loss in this way, the classic Shockley-Queisser limit for non-concentrating planar solar cells can be exceeded.\(^{90}\)

The above argument assumes no non-radiative losses. This is however hard to achieve in reality, even for high-quality III-V materials. Non-radiative losses lowers the open circuit voltage according to

\[ V_{OC} = V_{OC}^{\text{rad}} - kT \ln(QE_{ext}) \quad \text{(eq. 3.5)} \]

where \( QE_{ext} \) is the external quantum efficiency, i.e. the ratio of radiative recombination to the total recombination. To minimize the effect of non-radiative recombination, the light should be extracted from the semiconductor as efficiently as possible, minimizing the risk of trapped light bouncing around until it is absorbed and the carriers go through non-radiative recombination. Nanowire arrays have been demonstrated to improve the extraction efficiency\(^{94}\) and in contrast to traditional planar cells, can have both an emission angle restriction and improved extraction efficiency.\(^{91}\) In addition, axial nanowire arrays have an absorption cross-section larger than the p-n junction area. Since non-radiative recombination often scales with the p-n junction area, this has a potential to boost \( V_{oc} \) also in the non-radiative limit.\(^{88}\)

To summarize, nanowire solar cells can potentially increase the open-circuit voltage in both the radiative and non-radiative limit: By restriction of the emission angle in the radiative recombination limit, and by improving extraction efficiency and decreasing the probability of non-radiative recombination in the non-radiative limit. These effects together with the potential reduction in material usage and the strain-accommodation that makes it possible to grow new heteroepitaxial material.
combinations for multi-junction photovoltaics\textsuperscript{95}, make nanowires very attractive for high-efficiency solar cells. Several groups have demonstrated nanowire solar cells in different material systems\textsuperscript{28,87,88,95–100} and the record conversion efficiencies are increasing rapidly\textsuperscript{87,88}. Key factors to control in order to attain high efficiency are doping and surface properties, which both depend on reliable electrical characterization.

3.2 Light emitting diodes

An LED is the reciprocal of a solar cell. It converts electrical energy directly to light by recombination of electrons and holes. Most commonly, an LED is based on a p-n junction. Electrical contacts are placed on each side of the p-n junction and a forward voltage is applied to inject carriers in the junction. When the injected electrons and holes meet, they can recombine radiatively and emit light with a wavelength corresponding to their energy difference, i.e. the band gap.

There are three basic types of recombination for an electron-hole pair: radiative recombination over the band gap, trap-induced non-radiative recombination Shockley-Read-Hall (SRH) and Auger recombination (figure 3.2). These recombination mechanisms compete in semiconductor materials and to achieve high efficiency it is critical to design the LED so that radiative recombination is the dominating mechanism.

![Figure 3.2. Recombination processes in a semiconductor.](image)

Since radiative recombination requires an electron and a hole to meet, the probability of a radiative recombination event is proportional to the product of the density of electrons (n) and holes (p). Trap-induced SRH recombination can be thought of as a carrier falling into a trap energy level within the bandgap and then in a second step falling down to the lower energy band and completing the recombination. SRH
recombination is proportional to the carrier density and trap density. In Auger recombination, an electron and hole recombine over the band gap, but instead of emitting energy in form of a photon, the energy is transferred to another electron or hole. Since this is a three-particle event, the probability is proportional to a product with the cube of the carrier density as unit. We can express the recombination rate as

$$R_{\text{recombination}} = An + Bnp + Cn^2p$$

(eq. 3.6)

where $A$, $B$ and $C$ are coefficients for SRH, radiative and Auger recombination respectively. Often for semiconductors $A \gg B \gg C$, so SRH recombination dominates for low carrier density, radiative recombination dominates for medium carrier density and Auger may have a significant impact at very high carrier concentrations. An important factor for a high radiative coefficient is a direct band gap. In nitride LEDs, excitonic recombination is a significant part of the radiative recombination.\textsuperscript{101} For most other III-V materials, free carrier recombination dominates.\textsuperscript{101}

A sketched band diagram of an LED is shown in figure 3.3. In order to increase the probability of radiative recombination in LEDs, quantum wells are inserted in the p-n junction to confine carriers and locally increase the carrier density. By controlling the material composition and size of the quantum wells it is also possible to control the energy levels and thus the emission wavelength. To stop electrons from flowing past the p-n junction without recombining in the quantum well, a short segment of electron blocking high band gap material is often inserted on the p-side of the p-n junction. It is usually not necessary to have such a blocking layer for the holes due to their lower mobility.

![Figure 3.3. Sketched band diagram of a light-emitting diode.](image)

The IV characteristic of an LED can also be described by the diode equation. However, a real diode often also has a parallel shunt path for the current and a series resistance. This can be expressed as:
where \( R_p \) and \( R_s \) is the shunt resistance and series resistance respectively. The IV characteristic of a diode with these parasitic resistances is shown in Figure 3.4. At low voltage the parallel shunt resistance dominates, at intermediate voltage the exponential dominates, and at high voltage the series resistance dominates.

The IV characteristic can give important information about an LED. Series resistance can be caused for example by contact resistance or resistance in the neutral regions. A parallel shunt path can be caused by imperfections in the p-n junction.

Another important parameter is the ideality factor. The ideality factor describes the deviation of the exponential diode IV characteristic from an ideal diode. In a device with no recombination in the depletion region, the carrier transport is dominated by diffusion current, which is determined by the minority carrier concentration at the end of depletion region. This injected carrier concentration is proportional to \( \exp(eV/(kT)) \), so naturally the current has the same dependence, i.e. \( n = 1 \). However, if the carriers instead recombine in the depletion region, the current is driven by resupply of recombined carriers and therefore limited by the recombination rate. The recombination rate is proportional to the carrier density (eq. 3.6), so this current must also have an exponential dependence. However, since different recombination mechanisms have different carrier concentration dependence, they will also lead to different voltage dependence, i.e. ideality factor. SRH recombination is most probable to take place where the electron and hole quasi Fermi-level, i.e. the two carrier densities are proportional to \( \exp(eV/(2kT)) \) and the ideality factor equals two. These two cases were discussed by Sah, Noyce and Shockley in a classic paper from 1957. However, in modern LEDs the situation is different and ideality factors larger than two are often observed. Radiative recombination dominates and the
recombination primarily takes place in a quantum well. In addition, GaN LEDs typically have higher doping on the p-side but still low hole concentration due to the large activation energy of the p-type Mg dopant. This makes the p-n junction asymmetric and the rate-limiting carrier concentration may be modulated more weakly by the applied voltage, leading to an ideality factor larger than 2. Other theories to explain the high ideality factors in GaN LEDs include Schottky contacts and tunneling current.

3.3 Nitride LEDs

The (Al)(In)GaN material system is very well suited for use in LEDs. The band gap is direct and tunable from 6 eV for AlN to around 0.7 eV for InN, meaning that the emission can be tuned all the way from deep ultraviolet to infrared and cover the entire visible spectrum. However, there are a number of challenges when working with nitrides.

First, synthesizing bulk GaN is a very costly process and large wafers are not yet commercially available. Instead, most GaN substrates are made by growing GaN on a foreign material such as sapphire, SiC or silicon. These materials have different lattice parameters and thermal expansion coefficients than GaN, giving rise to strain and many defects, which in turn leads to threading dislocations. The dislocation density is often as high as $10^7$-$10^9$ cm$^{-2}$ for GaN on SiC or sapphire wafers. Dislocations serve as non-radiative recombination centers and often give rise to n-type conductivity.

Second, GaN is not symmetric along the most commonly used crystal orientation, the c-axis. The polarization stems from the difference in electro-negativity between the group III and group V atoms and results in polarization charges and an internal electric field. In addition to this spontaneous polarization, piezoelectric charges are also induced when the material is strained, e.g. at heterojunctions. The polarization effects are deleterious to the recombination efficiency in quantum wells because the internal fields separate the electrons and holes spatially, reducing the probability of radiative recombination (figure 3.5). This effect, called quantum-confined Stark effect (QCSE), is one of the most important challenges in LED development today. In particular, it has a large impact on the efficiency of green and red LEDs with high In content, and thus strain, in the quantum wells.
Third, it is challenging to grow InGaN alloys with sufficiently high quality. Due to the high vapor pressure of In, relatively low temperatures are needed to achieve films with high In composition in MOVPE. This may lead to introduction of point defects and poor quality. In addition, most InGaN alloys are thermodynamically unstable at the commonly used growth temperatures due to the large difference in interatomic spacing between GaN and InGaN. Therefore, films of InGaN are prone to phase separation. Due to these challenges, red and green nitride LEDs are grown with GaN buffer layers, leading to very poor performance because of the strong QCSE in the quantum wells and dislocations caused by the lattice mismatch. Dislocations have also been linked to exacerbating the phase separation. It should be noted that some phase separation of indium could create potential minima in the electronic structure, thus preventing carriers from reaching the dislocations. This is often cited as part of the reason it is possible to reach so high efficiency for blue InGaN LEDs, despite the high dislocation densities.

Fourth, achieving p-type conductivity in GaN is not straightforward. The most commonly used p-type doping is Magnesium. During the hydrogen-rich MOVPE process, the Mg acceptors form electrically inactive complexes with hydrogen. The complexes can be dissociated by electron beam irradiation or annealing at temperatures around 700 °C to give electrically active acceptors. However, even after this treatment, the activation energy of the acceptors is high, around 170 meV, resulting in an ionization rate below 1%. The p-type conductivity is thus often a limiting factor for GaN devices.

Last, GaN LEDs suffer from efficiency droop at high injection currents. The origin of this droop has been widely discussed, but is most likely due to increasing Auger recombination when the injected carrier density in the quantum wells is very high.

Despite these challenges, nitride LEDs emitting in near UV and blue with very high efficiencies (figure 3.6) are mass-produced. Achieving similar efficiencies for red, green and UV light would revolutionize the industry and open up many new possibilities for RGB color mixing for general illumination, efficient displays, water
purification etc. Reaching high efficiency in UV is hindered primarily by the high concentration of dislocations, low p-type conductivity of AlGaN and low light extraction efficiency.\textsuperscript{114} The efficiency for green and red light is limited by low radiative recombination probability due to strong QCSE and high defect density when the quantum well has high In composition and therefore is heavily strained.\textsuperscript{47,115}

![Figure 3.6. Experimental external quantum efficiency vs. wavelength. Data from \textsuperscript{116} and \textsuperscript{117}.](image)

Nanostructures offer many new opportunities to solve the challenges that face nitride optoelectronics.\textsuperscript{47,118,119} In particular, the unique strain relaxation and dislocation elimination effects mean that nanowires can be free from dislocations in the active region. Nanowires can also be used as dislocation-free substrates for growth of LEDs on the non-polar m-plane, thereby alleviating the problems associated with QCSE. This geometry also has the advantage of a large surface-to-volume ratio, which could reduce the current density in the active region and thus the problems with droop. Several groups have demonstrated nanowire LEDs\textsuperscript{21–24,118,120–129} and there is also corporate research\textsuperscript{129} and many patents on the topic.

Even though GaN nanowire LEDs utilizing the non-polar m-plane have the advantage of reduced quantum well polarization, it has been hard to achieve high material quality with high enough In composition\textsuperscript{47} and to incorporate In evenly in the quantum wells\textsuperscript{130} on this crystal plane. It is also challenging to grow InGaN nanowires by MOVPE, so green and red nitride LEDs are still most often grown from GaN nanowires, leading to strain and possibly defects in the active region. It is however possible to grow InGaN nano-pyramids with high In composition and material quality (paper IX).

Platelet technology combines many of the advantages of nanostructures with the benefits of conventional c-plane epitaxy. Platelets are created by first growing dislocation-free pyramid-shaped nanocrystals and then reshaping them in the growth
reactor to form a smooth top facet c-plane. This enables growth of c-plane active layers on dislocation-free, relaxed GaN and InGaN templates. If In-rich quantum wells are grown on relaxed InGaN barrier layers, strain and polarization is decreased significantly, leading to improved efficiency for green and red emission. Dislocation-free GaN is highly interesting for UV LEDs and electronic devices (paper VI).
4. Doping characterization at the nanoscale

In this chapter, the most commonly used electrical characterization techniques for nanowires are described and the content of the first four papers of the dissertation is discussed.

Parts of this chapter can be found in a slightly more comprehensive version in the book chapter Hall effect measurements in nanowires in 21st Century Handbook of Nanoscience (paper XI) and in my licentiate thesis from 2016: A Guide to Electrical Characterization of Semiconductor Nanowires.

4.1 Fabrication of nanowire Hall devices

The most common way to measure Hall effect in a nanowire, is to place contacts at each end of the nanowire to feed a current and on the side facets of the nanowire to measure the Hall voltage. The basic steps of fabricating such a device will be outlined here. Figure 4.1 shows a sketch of the fabrication process and figure 4.2 shows scanning electron microscope (SEM) images of the process.

First, the nanowires are transferred from the growth substrate to a substrate more suitable for measurements (figure 4.1a, 4.2a). The measurement substrate in this case is a doped Si chip covered with 100 nm SiO₂ and 10 nm of HfO₂. Both oxides provide electric insulation and the latter is added for its resistance to etching. Pre-patterned on the measurement substrate are metallic contact pads and alignment markers (figure 4.2a). The transfer of nanowires to the measurement substrate is done by rubbing a small piece of cleanroom tissue first on the growth substrate and then on the measurement substrate. This results in a large number of nanowires dispersed in random orientations over a relatively large area on the measurement substrate (figure 4.1a and 4.2b). When working with large diameter nanowires, a thin polymer spacer layer is spin coated on the chip after deposition of the nanowires in order to lift and stabilize the contacts, making it possible to use thin and narrow contacts even on a larger nanowire. The spacer layer is designed to just barely cover the nanowires (figure 4.1b). A suitable mix for nanowires with a diameter around 200 nm is S1805:PGMA
(1:1). To remove the thin polymer on top of the nanowires and open up for the contacts, the sample is etched in oxygen plasma (figure 4.1c and 4.2c).

The position of the nanowires is determined with respect to the alignment markers (figure 4.2b inset) using scanning electron microscopy. Electrical contacts can then be designed and exposed in PMMA resist using electron beam lithography (EBL) (figure 4.1d). After the EBL exposure, the sample is etched to remove native oxide from the nanowire surface and metal is deposited to form the contacts. Excess metal is removed in a liftoff process (figure 4.1e and 4.2d). Further functionality can be added to the nanowire device by depositing a gate oxide using atomic layer deposition and defining a gate electrode using EBL and thermal evaporation.

This method is very versatile and can be used to make devices for many different applications. The constraints to the contact design mainly lie in the resolution and
overlay accuracy of the EBL. With a good EBL system it is possible to fabricate devices with contact spacing down to a few tens of nanometers. The alignment precision of the contacts is also on the order of tens of nanometers.

Other groups have taken different approaches to the fabrication of nanowire Hall devices. Blömers et al.\textsuperscript{63} fabricated InAs nanowire Hall devices without a spacer layer. DeGrave et al.\textsuperscript{64} used tilted evaporation to fabricate nanowire Hall devices with a slight contact offset, but much relaxed lithographic constraints. Murata et al. used focused ion beam to deposit contacts.\textsuperscript{67}

\textbf{Figure 4.2.} SEM images of nanowire device fabrication. a) Overview image of measurement substrate. b) Overview of one write field. The bond pads can be seen in the corners of the image. Inset: Magnified alignment marker (scale bar 5 µm). c) Nanowire surrounded by etched spacer layer. d) Finished nanowire device.
4.1.1 Metal-semiconductor contacts

The contact is often one of the most critical parts of a nanowire device. Ideally, the contact should have low resistance and Ohmic (linear) IV characteristics. In a very simple model, an Ohmic contact can be made by matching the semiconductor work function ($\phi_s$) to the metal work function ($\phi_m$) (figure 4.3a). The work functions are defined as the difference between the vacuum energy and the Fermi level. If the work functions are not matched, mobile charge will flow over the interface leaving a space charge region in the semiconductor and forming a potential barrier (Schottky barrier) (figure 4.3b). The band bending ($\phi_{bi}$) is equal to the difference between the work functions, $\phi_{bi} = \phi_m - \phi_s$. The barrier height is equal to the difference between the metal work function and the electron affinity of the semiconductor ($\chi_s$), $\phi_b = \phi_m - \chi_s$.

![Figure 4.3. Metal-semiconductor contact. a) The metal and semiconductor are not in contact. The metal work function and semiconductor work function are not aligned. b) The metal and semiconductor are put in contact. Mobile charge flows over the interface until equilibrium is reached and a space charge region has formed. The space charge leads to band bending in the semiconductor and a Schottky barrier at the interface.](image)

The current transport over a Schottky barrier in a low-doped semiconductor is dominated by thermionic emission. Due to the asymmetry of the barrier and the thermal distribution of carriers, a Schottky contact has rectifying and non-linear IV characteristics. This can be a problem when characterizing nanowire devices, since it may be hard to separate the contact characteristics from the nanowire characteristics. However, if the doping level in the semiconductor is high, the space charge region becomes thin and tunneling current through the barrier can lead to Ohmic characteristics despite the presence of a barrier. Highly doped contact segments are therefore often used to improve the contact properties (paper III).

This simple model is accurate for clean, defect free, perfectly terminated semiconductors. However, almost all semiconductors have defects such as dangling bonds and native oxides on the surface. These defects often create new energy states
within the band gap and may cause pinning of the Fermi level and a surface band bending. E.g. in InAs, the Fermi level may be pinned in the conduction band, causing a surface accumulation layer.\textsuperscript{131} In GaN, the Fermi level may be pinned inside the band gap causing a surface depletion layer.\textsuperscript{73}

A native oxide on the semiconductor surface may form an insulating layer between the metal and the semiconductor. The oxide can often be removed by wet etching the sample just before deposition of the contact metal.

To further improve the contact properties it is possible to anneal the contacts. However, when the temperature is increased, many different processes may be at play. The processes are very different in different material systems, but often involve diffusion of contact material into the semiconductor, diffusion of semiconductor material into the contact and formation of new alloys in the metal-semiconductor interface.\textsuperscript{132,133} These processes are hard to predict and may affect the properties of the semiconductor. Contact annealing should therefore be evaluated carefully before use on nanoscale characterization devices.

### 4.2 Simulation of electric transport

Nanostructures often have complex shapes and geometries that are challenging or impossible to represent accurately using simple analytic models. In addition, the electric contacts often cover a relatively large part of the device, making the traditional assumption of point-like contacts inaccurate. For a more accurate representation, finite element method (FEM) simulations can be used to simulate the potential and currents in a nanostructure. FEM is a powerful tool where semiconductor transport equations can be solved in an arbitrary geometry. Most of the nanostructures studied in this dissertation are large enough not to exhibit any significant quantum confinement effects for the charge carriers, so their properties can be described by semi-classical 3D models. To simulate transport and carrier concentrations in the quantum wells present in LEDs, other methods are needed.

To model the carrier transport, we use the fact that electric charge is a conserved quantity, i.e. it cannot be generated or simply vanish (without this being accounted for in a generation or recombination process). This gives us the current continuity equation

\[
\nabla \cdot \mathbf{J} = -\frac{\partial \rho}{\partial t} \quad (\text{eq. 4.1})
\]

where \(\rho\) is the charge density. This states that the charge in a point does not change unless there is a difference in the current going in and out of the point.

The current in a semiconductor can be described by drift and diffusion. Drift current is due to the electrons’ response to an electric field, while diffusion current is
caused by diffusion of carriers between areas with different carrier densities. The drift and diffusion currents for electrons can be written as

\[ \mathbf{J}_n = q n \mu_n \mathbf{E} + \mu_n kT \frac{dn}{dr} \]  
(eq. 4.2)

where \( q \) is the electron charge, \( n \) is the electron density, \( \mu_n \) is the electron mobility, \( \mathbf{E} \) is the electric field, \( k \) is the Boltzmann constant, \( T \) is the temperature and \( \frac{dn}{dr} \) describes the carrier density gradient. The hole current is defined correspondingly. In some cases, a semiconductor device can be considered to have an isotropic carrier density and be modeled by just the current continuity equation and drift current (the first term in the equation above). In some cases, it is however necessary to consider differences in charge carrier concentration and potential. This can be calculated using another divergence theorem, Poisson’s equation. This equation states that the electric flux density through a closed surface is proportional to the electric charge inside the surface.

\[ \nabla^2 \psi = -\frac{\rho}{\varepsilon}. \]  
(eq. 4.3)

where \( \psi \) is the electric potential, \( \varepsilon \) is the permittivity and \( \rho \) is the electric charge density. The charge carrier density in a semiconductor is in turn described by

\[ n = \int g(E) f_{FD} dE \]  
(eq. 4.4)

where \( g(E) \) is the density of states and \( f_{FD} \) is the Fermi distribution.

The electronic structure and distribution of charge carriers, the drift-diffusion equations, the current continuity equation, and Poisson’s equation constitute a semiclassical framework for calculations of electric transport in most 3D semiconductor devices. It gives us the means to calculate charge distribution, currents and potentials in our devices – a powerful and very important tool to understand and analyze the results from electrical characterization.

### 4.3 Hall effect characterization

A charge carrier subjected to a magnetic field perpendicular to the direction of its movement is deflected from its path as described by the Lorentz force. Already in 1879, Edwin Hall realized that also charges moving in a conductor are deflected by magnetic fields and started investigating the effect that was later named after him. Figure 4.4 illustrates the Hall effect. A current is conducted through a semiconductor sample while a magnetic field \( (B) \) is applied in a direction \( (z) \) perpendicular to the direction of the current \( (x) \). A force will then act on the carriers in a third direction \( (y) \). This causes a
displacement of charge and a counter-acting electric field is created in the y direction. This electric field can be measured as a voltage in the y direction, the Hall voltage (\(V_H\)). The Hall voltage is inversely proportional to the carrier concentration.

![Figure 4.4](image)

Figure 4.4. The Hall effect in a cylindrical structure. Charge carriers are deflected in a direction perpendicular to the current and the magnetic field.

The Hall effect in a cylinder can be described by an analytic expression by assuming that the contacts are point-like, i.e. that they are located at the edge of the sample and that their extension is negligible compared to the width of the sample. This approximation is not true for a typical nanowire Hall device, and the real geometry should be accounted for to determine the charge carrier concentration accurately. This can be done by implementing a finite element method model solving the drift current equation, \(J = \sigma E\) and the current continuity equation. To describe the carrier displacement due to the Lorentz force, we derive the anisotropic conductivity tensor, \(\sigma\) for the case of an extrinsic semiconductor where the carrier scattering time (\(\tau\)) is independent of energy. This model was presented in \(^{62}\).

The motion of an electron can be described by

\[
F = m^* a = m^* \left( \frac{dw}{dt} + \frac{v}{\tau} \right) = qE + qv \times B. \quad (eq. \ 4.5)
\]

where \(m^*\) is the effective mass, \(a\) is the carrier acceleration and \(v\) is the carrier velocity. If the magnetic field is applied in the z-direction, \(B = (0,0,B)\), the equation can be separated into the spatial components

\[
m^* \left( \frac{dv_z}{dt} + \frac{v}{\tau} \right) = q(E_x + v_y B) \quad (eq. \ 4.6)
\]
\[ m^* \left( \frac{dv_y}{dt} + \frac{v_x}{\tau} \right) = q(E_y - v_x B) \quad (\text{eq. 4.7}) \]
\[ m^* \left( \frac{dv_x}{dt} + \frac{v_y}{\tau} \right) = qE_z. \quad (\text{eq. 4.8}) \]

In steady state, \( dv/dt = 0 \). Solving for \( v \), we get
\[ v_x = \frac{\frac{m^*}{q} E_x + \frac{m^*}{q} E_y B}{1 + \left( \frac{m^*}{q} B \right)^2} \quad (\text{eq. 4.9}) \]
\[ v_y = \frac{\frac{m^*}{q} E_y - \frac{m^*}{q} E_x B}{1 + \left( \frac{m^*}{q} B \right)^2} \quad (\text{eq. 4.10}) \]
\[ v_z = \frac{q}{m^*} E_z. \quad (\text{eq. 4.11}) \]

Since \( \mathbf{J}_{\text{n,drift}} = \mathbf{v} e n = \mathbf{\sigma} \mathbf{E} \), the above equations can be expressed in the conductivity tensor
\[
\mathbf{\sigma} = \sigma_0 \begin{pmatrix}
1 & \frac{q_x B}{m^*} & 0 \\
\frac{q_y B}{m^*} & 1 + \left( \frac{m^*}{q} B \right)^2 & 0 \\
0 & \frac{q_z B}{m^*} & 1 + \left( \frac{m^*}{q} B \right)^2
\end{pmatrix} \quad (\text{eq. 4.12})
\]

where \( \sigma_0 = \frac{q^2 \tau n}{m^*} \).

By using the conductivity tensor in the relation \( \mathbf{J}_{\text{n,drift}} = \mathbf{\sigma} \mathbf{E} \) we can simulate the Hall effect in virtually any semiconductor structure using a FEM software, such as COMSOL Multiphysics and thus determine the charge carrier concentration from a Hall effect measurement.

Other authors have taken slightly different approaches to modeling the Hall effect in nanowires. Barbut et al.\(^\text{135}\) pointed out that a contact may introduce a shunt path for the current along the nanowire and influence the measurement. Fernandes et al.\(^\text{136}\) showed that diffusion current could reduce the Hall voltage in nanowires with a radius approaching the Debye screening length, since diffusion currents may prevent the formation of charge buildup at the edges of the sample. If not accounted for, this effect could lead to an overestimation of the carrier concentration. Murata et al.\(^\text{68}\) carried out detailed modeling of the Hall effect in their bismuth nanowire system, including effects of the band structure and different scattering mechanisms. The modeling presented here could certainly be expanded by accounting for more effects, such as more realistic contacts and surface phenomena. However, such input parameters are rarely well-known and must therefore often be experimentally determined for the devices in question. Which effects should be considered will differ very much between different devices and material systems. In principle, all kinds of characterization should assess the system as a whole and identify dominating effects that should be accounted for.
4.4 Field-effect characterization

The principle of field-effect characterization is to fabricate a nanowire FET and measure the transconductance, i.e. how the conductivity changes when the charge in the transistor channel is modulated by the gate voltage. If the capacitive coupling between the gate and the nanowire is known, this gives us the charge carrier mobility. When the mobility is known, the charge carrier concentration can be determined from the conductivity. The simplest way to fabricate a nanowire FET is to place a nanowire on an oxide-covered conductive chip covered serving as a back gate, and put source and drain contacts at each end of the nanowire. Such a device is illustrated in figure 4.5.

![Back gated nanowire field-effect transistor.](image)

A simple model for a nanowire transistor can be derived from the Drude model definition of conductivity ($\sigma$)

$$\sigma = ne\mu$$  \hspace{1cm} (eq. 4.13)

where $n$ is the charge carrier concentration, $e$ is the elementary charge and $\mu$ is the mobility. The conductivity can also be expressed by rewriting Ohm’s law as

$$\sigma = \frac{dI_{SD}}{dV_{SD}} \frac{L}{A}$$  \hspace{1cm} (eq. 4.14)

where $I_{SD}$ and $V_{SD}$ are the source-drain current and voltage, respectively. $L$ is the channel length and $A$ is the cross section area of the nanowire. The charge carrier concentration is controlled by the gate with the relation $nV/e = C(V_G - V_{threshold})$, where $V$ is the volume of the nanowire channel, $C$ is the capacitance between the nanowire and the gate ($C \equiv dQ/dV_G$), and $V_{threshold}$ is the applied gate voltage where the nanowire is fully depleted. Combining this gives us

$$\frac{dI_{SD}}{dV_{SD}} = \frac{C(V_G - V_{threshold})\mu}{L^2}$$  \hspace{1cm} (eq. 4.15)

or alternatively, by integrating with respect to $V_{SD}$ and differentiating by $V_G$
\[
\frac{dI_{SD}}{dV_G} = \frac{C \mu V_{SD}}{L^2}. \quad \text{(eq. 4.16)}
\]

These equations can be used to extract the mobility from a transconductance measurement.

This simple model has been widely used, although it has a number of limitations that are not always addressed. First, calculating the capacitance in a semiconductor, in contrast to a metallic system is not merely a geometric problem, but also the electronic structure of the semiconductor and the surface properties should be accounted for. Second, not accounting for the contact resistance may introduce a significant error. These two issues will be further discussed in the following sections. In addition, a semiconductor can only be depleted relatively close to the gate. When the applied gate voltage causes a band bending of about the same size as the band gap, minority charge carriers will accumulate at the gate interface stopping further expansion of the depletion area and the semiconductor is said to be in strong inversion. By defining the onset of strong inversion as

\[
E_V(\text{surface}) - E_F = E_F - E_C(\text{bulk}) \quad \text{(eq. 4.17)}
\]

we can solve for the maximum depletion width \((w_D)\) with Poisson’s equation (using the full-depletion approximation)

\[
w_D = \sqrt{\frac{2e}{\varepsilon^2 \psi_{S,inv} N_D}} \quad \text{(eq. 4.18)}
\]

where \(\psi_{S,inv}\) is the band bending at the surface at the onset of strong inversion and \(N_D\) is the donor density. The maximum depletion width as function of donor density for n-InP is plotted in figure 4.6.

![Figure 4.6. Maximum depletion width in a 1D InP MOS structure.](image-url)
It can be seen that the maximum depletion width decreases with increasing doping and that it is only about 30 nm at a donor density of $10^{18}$ cm$^{-3}$. This simple calculation shows that only nanowires with low doping or small diameter can be fully depleted.

### 4.4.1 Gate capacitance

The simplest and most common way to estimate the gate capacitance of a back-gated nanowire FET is to use the analytic expression for an infinitely long metal cylinder on a plane, giving the capacitance

$$\frac{C}{L} = \frac{2\pi \varepsilon}{\tanh(\frac{r}{\varepsilon})} \quad \text{(eq. 4.19)}$$

where $\varepsilon$ is the dielectric constant of the gate oxide, $r$ is the radius of the nanowire and $h$ is the gate oxide thickness. Besides assuming the nanowire is infinitely long, this model also assumes that the nanowire is fully covered in a dielectric with the same dielectric constant $\varepsilon$, which is usually not the case for real devices.

Aside from the error introduced by the approximation of the geometry, there is another limitation to the accuracy of this model. The gate capacitance in a semiconductor is really the series combination of the oxide capacitance and the semiconductor capacitance.

$$C_G = \frac{C_{OX}C_S}{C_{OX} + C_S}, \quad \text{(eq. 4.20)}$$

where $C_G$ is the gate capacitance, $C_{OX}$ is the oxide capacitance and $C_S$ is the semiconductor capacitance. In the model above, only $C_{OX}$ is considered. As long as $C_S$ is much larger than $C_{OX}$, $C_G$ will be approximately equal to $C_{OX}$, but for thin gate oxides, $C_S$ may decrease the gate capacitance significantly. The semiconductor capacitance also decreases when the depletion region below the gate expands, which may cause the effective capacitance to change throughout a gate sweep.

To account for both the true geometry and the semiconductor capacitance, a 3D finite element method model using Poisson’s equation and Fermi-Dirac statistics can be used. By solving for the carrier density in the nanowire at different gate voltages, the capacitance can be extracted from the change in space charge,

$$C = \frac{dQ}{dV_G} \quad \text{(eq. 4.21)}$$

where

$$Q = e \int\int\int (N_D - n + p) \, dx dy dz. \quad \text{(eq. 4.22)}$$
$N_D$ is the donor concentration, $n$ is the electron concentration in the conduction band and $p$ is the hole concentration in the valence band. The potential profile and charge distribution from such a simulation can be seen in figure 4.7. The analytic expression for a cylinder-plane system overestimates the gate capacitance of a back-gated nanowire transistor (without a spacer layer) by about a factor of two, compared to this model\textsuperscript{57}, leading to an overestimation of the carrier concentration. A comparison between the analytic expressions and a simulated device with a polymer spacer layer can be found in paper III.

![Figure 4.7. Simulation of capacitance in a nanowire FET using FEM. Potential (a) and net charge density (b) for a back-gated InP NW FET with an applied gate voltage of -3V. The nanowire diameter is 100 nm and the donor concentration is $10^{18}$ cm$^{-3}$.](image)

### 4.4.2 Surface states

The band structure of a semiconductor is a consequence of the periodic crystal structure. At a semiconductor surface the crystal structure is disturbed, e.g. by dangling electron bonds or by bonds to a surface oxide. These disturbances create new energy states that typically appear in or near the band gap. These charged surface states cause an opposing space charge layer and thus band bending in the semiconductor. The surface states can either be negatively charged when filled and neutral when empty (acceptor-like) or positively charged when empty and neutral when filled (donor-like). Thus, the density of surface states and the Fermi level of the semiconductor control the amount of charge at the surface. From this model, it can be assumed that if the Fermi level is at a certain point, the charges of the surface states cancel, i.e. the net surface charge is zero. This point is called the charge neutrality level, $E_{NL}$. Assuming a constant surface state density, the surface charge is then proportional to the deviation between the Fermi level and the neutrality level

$$\sigma_s = qD_s(E_{NL} - E_F). \quad (eq. 4.23)$$
If $D_s$ is large, the charge accumulation will make the bands bend so that the charge neutrality level is close to the Fermi level, thus pinning the Fermi level.

With surface states, the effective capacitance of the FET is reduced and the extracted mobility values may be inaccurate. In extreme cases, the nanowire transistor may not respond to gate voltage changes at all. In figure 4.8, the reduction in effective capacitance of a NW FET for different surface state densities is shown normalized to the capacitance for $D_s = 0$. The capacitance was calculated with the model described in the previous section, modified to include surface states. Apart from the strong reduction in capacitance for high $D_s$, it can be seen that a thin top gate is less sensitive to higher surface state densities compared to a back gate. This difference in coupling can in some cases be used to determine $D_s$.

![Figure 4.8. Reduction in capacitance with surface states. Capacitance for an InP nanowire ($r = 100$ nm) with a charge neutrality level 0.74 eV above the valence band, normalized to the capacitance when $D_s = 0$. The top gate dielectric was 11 nm and the back gate dielectric 100 nm.](image)

### 4.4.3 Contact resistance

All nanowire FETs have contact resistance. In some cases, this affects the quantification of mobility and charge carrier concentration significantly.

Consider a nanowire FET in which the source and drain contacts have a contact resistance of $R_C/2$ each. We describe the channel resistance as a function of the amount of mobile charge and the mobility in the channel:

$$\sigma = \frac{1}{\rho} = ne\mu = \frac{L}{AR}$$

(eq. 4.24)
\[ R_{NW} = \frac{L}{Ane\mu} = \frac{L}{Ae\mu(n_0 + CV_G/eLA)} \]  

(eq. 4.25)

where \( n_0 \) is the carrier concentration at \( V_G = 0 \) and \( CV_G/(eLA) \) is the carrier density induced by the gate. The total resistance of a system with resistors connected in series is the sum of resistances. The total conductance for the nanowire and the contact resistances is thus

\[ \frac{dI_{SD}}{dV_{SD}} = \left( R_C + \frac{L}{Ae\mu(n_0 + CV_G/eLA)} \right)^{-1}. \]

(eq. 4.26)

The transfer characteristic for a typical InP n-type NW FET modeled by the above equation with a few different contact resistances are shown in figure 4.9. Introducing a contact resistance of about the same size as the channel resistance changes the transconductance significantly. However, when a gate voltage is applied so that the channel is almost depleted (around -10V in figure 4.9), the contact resistance becomes small compared to the channel resistance. In this regime, the contact resistance can be neglected and the mobility can be determined using the equations in the previous section or more accurately by fitting the parameters of the above equation to the measured data.  

\[ R_C = 0 \Omega \quad R_C = 2000 \Omega \quad R_C = 5000 \Omega \]

Figure 4.9. Calculated transfer characteristic (a) and transconductance (b) for InP NW FETs with different contact resistances.

Nanowires intended for electro-optical applications, such as solar cells and LEDs, usually have relatively large diameter and are heavily doped, and thus not possible to deplete fully. We rewrite the equation above to get simpler expression for this case. By integrating with \( V_{SD} \) and differentiating by \( V_G \) we get

\[ \frac{dI_{SD}}{dV_G} = \left( R_C + \frac{L}{Ae\mu(n_0 + CV_G/eLA)} \right)^{-2} \frac{L}{(Ae\mu(n_0 + CV_G/eLA))^2} \frac{\mu C}{L} V_{SD}. \]

(eq. 4.27)
This expression can be simplified by assuming that the charge density induced by the gate is small compared to the carrier concentration with no applied gate voltage, \( n_0 \gg CV_G/(eLA) \). This is accurate for large diameter and heavily doped nanowire FETs at small gate voltages. By also introducing the resistance of the nanowire with no applied gate bias

\[
R_{NW0} = \frac{L}{\kappa e \mu n_0} \quad (eq. 4.28)
\]

we get

\[
\frac{dI_{SD}}{dV_G} = \frac{1}{\left( \frac{R_C}{R_{NW0}} + 1 \right)^2 \mu C L^2 V_{SD}} \quad (eq. 4.29)
\]

or equivalently, by introducing \( V_{SD} = I_{SD}(R_C + R_{NW}) \) and

\[
\mu = \frac{1}{\rho ne} = \frac{L}{R_{NW0} A n_0 e} \quad (eq. 4.30)
\]

\[
\frac{dI_{SD}}{dV_G} = \frac{1}{\left( \frac{R_C}{R_{NW0}} + 1 \right) L n_0 e A} \quad (eq. 4.31)
\]

With this model, it is possible to extract mobility and carrier concentration from field-effect measurements on nanowire FETs with contact resistance even if they cannot be fully depleted. It is however important to keep in mind that it is only the volume of the nanowire that can be depleted that is actually characterized. The model presented here was derived and used in paper III. Note that this model assumes that the effect of offset of the actual source potential to the gate potential due to the source contact resistance is negligible \( (R_{c,source}dI_{SD}/dV_G \ll 1) \), as is the case for these nanowire devices. A model accounting for this effect is derived in ref \(^{138}\) and ref \(^{139}\).

### 4.5 Hall effect characterization of InP core-shell nanowires (paper I and II)

In paper I, Hall effect measurements were carried out on two series of InP core-shell nanowires to map out doping concentrations for different dopant (TESn) flows and III/V ratios. The nanowires had p-type Zn-doped cores and heavily Sn-doped (n-type) shells. The total nanowire diameter was up to approximately 400 nm. This type of structure is ideal for Hall effect measurements. Since the contacts are placed on the n-type shell and the p-n junction blocks current from entering the p-type core, the shell can be characterized on its own. A nanowire contacted for Hall effect measurements is shown in figure 4.10a. To carry out a Hall effect measurement, current is sourced
through the outer contacts of the nanowire, the magnetic field is applied perpendicular to the substrate and the Hall voltage is measured between the contacts on the side facets of the nanowire. The device has three pairs of Hall contacts to enable measurements with spatial resolution along the length of the nanowire. The carrier concentration was extracted by measuring the size of the nanowires and positions of the Hall contacts from SEM images and then simulating the devices using the model previously described (figure 4.10b). Thanks to the spatial resolution of the measurements, a concentration gradient could be observed along the nanowire for certain growth conditions. The spatial resolution also made it possible to draw conclusions about the effect that the concentration of the dopant and growth precursors has on the formation of different crystal facets.

Figure 4.10. a) InP core-shell nanowire Hall device. b) Hall effect simulation in an hexagonal InP core-shell nanowire.

In paper II, nanowire Hall effect measurements were used as a reference to compare data from electrical characterization to data extracted from µ-photoluminescence (µ-PL) and cathodoluminescence (CL) measurements. The basic principles of these two optical characterization techniques are very similar; the charge carriers in the semiconductor are excited and when the carriers recombine, the emission spectrum is recorded. In µ-PL, a focused laser beam is used to excite the carriers, while an electron beam is used for CL.

The emission spectrum changes with the doping of the semiconductor and can therefore be used to quantify the charge carrier concentration. In an intrinsic material, the energy of the emission peak is given by the bandgap of the material, and the peak width is given by the temperature. For low doping concentrations, the emission peak shifts to a lower energy due to transitions via localized energy levels introduced by the dopants and the peak is widened. For high doping concentrations, the Fermi level moves up into the conduction (valence) band and the semiconductor becomes degenerate. Now, since all the states close to the band edge are filled, the emission is shifted to higher energy (similar to the Burstein-Moss effect). The peak becomes even
wider and the high-energy side of the peak reflects the Fermi distribution. In addition, by the introduction of new recombination pathways, new peaks may emerge with higher doping concentration, increasing the complexity of the spectrum. The best way to deduce the carrier concentration therefore depends on both the material system and the doping level. In paper II, the peak width is used to determine the charge carrier concentration at lower doping levels and a Fermi level fit is used to determine the charge carrier concentration at higher doping levels.

4.6 Experimental comparison between Hall effect and field-effect measurements (paper III)

The accuracy of field-effect characterization has been a hot topic in the nanowire research community for many years. For paper III, we designed a nanowire device to enable direct experimental comparison between Hall effect measurements and field-effect measurements on the same single nanowire. The device was designed with both a top gate and a back gate to further increase the measurement capabilities. Furthermore, devices with two different top gate oxide thicknesses were fabricated. These devices were used to study the doping concentration in a series of n-type InP nanowires with varying dopant flow (H₂S) at growth. The nanowires were synthesized with the VLS method from gold seed particles defined on an InP substrate by Nano Imprint Lithography. The nanowires had a diameter of approximately 200 nm and a total length of 2.5 µm. The nanowires had contact segments with higher doping level extending approximately 250 nm from each end to improve the contact properties.

A device is shown in figure 4.11a and a cross-section sketch in 4.11b.

Figure 4.11. a) Colorized SEM image of a device for characterization b) Schematic of the cross-section through the top gate of a device.
In figure 4.12a, Hall effect measurements are shown for three different nanowires grown with different dopant molar fractions. The slopes are steeper for lower dopant flow, just as expected. The doping levels were extracted by simulating the devices in the 3D FEM model previously described using the nanowire dimensions, geometry and position of the contacts as input.

The capacitances of the top-gate and the back-gate were also simulated by the FEM model previously described. Since the investigated nanowires have relatively large diameter and are heavily doped, only a fraction of the nanowire is actually depleted. It was also found that the capacitance was not constant throughout the gate sweep, especially for the thinnest gate oxide and lowest carrier concentration. A back-gate sweep is shown in figure 4.12b. It is clear that the nanowire is not depleted since the current does not approach zero, and therefore the contact resistance was extracted from four-probe resistivity measurements and accounted for using the expression previously derived.
Figure 4.13. Measured charge carrier concentration as function of dopant gas molar fraction. The error bars show the standard deviation between the extracted values from different devices. The number of measurement points per technique was: Hall: 28, Top gate 11nm: 12, Top gate 47 nm: 12, Back gate: 28.

Figure 4.13 shows the charge carrier concentration measured with the different techniques as function of the dopant molar fraction at growth. There is a clear trend with increasing charge carrier concentration for increasing dopant molar fraction. The concentrations measured with the different techniques are slightly scattered but agree relatively well. It is important to keep in mind that the Hall effect measurements measure the carrier concentration in the entire electrically active cross section of the nanowire, whereas the field-effect measurements only measure the properties in the limited depletion volume close to the gate. A radial variation in carrier concentration or mobility could therefore give a difference between the methods.

Another trend to note is that the data from the top gated measurements with 11 nm HfO₂ gate oxide are on the high side compared to the other techniques. Since the equivalent oxide thickness is so low for this device, a thin native oxide forming on the surface or a thin surface depletion region would make a significant difference for the gate capacitance. For the thicker gate oxides, such deviation from the ideal structure would have a much smaller effect on the gate capacitance. Another explanation for the higher values could be that the gate capacitance is changing throughout the measurement range. To account for this, the transconductance was not extracted with a linear fit as for the other devices, but instead by taking the peak value.

In summary, this comparison shows a relatively good correlation between the measurement techniques. For the field-effect measurements it is important to use a model accounting for the contact resistance and to calculate the gate capacitance properly. If this had been neglected, the carrier concentrations would have been about a factor of three higher for these particular devices. In addition, the field-effect devices
should be designed with a relatively thick gate oxide to minimize the effects of surface depletion layers, native oxide and non-constant capacitance in the gate voltage sweep range. It should also be noted that no correction was made for surface defects. The surface defect density for InP is usually considered to be relatively low, but has not been measured in these nanowires. If the surface defect density were high, it would cause a decrease in the effective gate capacitance and thus an overestimation of the carrier concentration extracted from the field-effect measurements. A moderate surface depletion would only have minor effect on the carrier concentration extracted from the Hall effect measurements.

In conclusion, Hall effect measurements have significant advantages when it comes to large diameter and heavily doped nanowires that cannot be fully depleted. Field-effect measurements however offer a simpler, surface sensitive evaluation that is especially interesting for thinner and less doped nanowires.
4.7 Three-probe Hall characterization (paper IV)

Hall effect characterization of nanowires is a rather time-consuming and challenging task due to the complexity of device fabrication and the difficulty in interpreting the measurements without FEM modeling. Additionally, the resolution of the lithography process to define contacts puts a limit to how thin nanowires can be contacted. In order to circumvent these limitations, a three-probe Hall effect characterization method is presented in paper IV. The principle of the three-probe Hall method is to measure the Hall voltage as the change in potential in a single contact as the strength of the applied magnetic field is varied instead of the traditional method of measuring the Hall voltage as the potential difference between two contacts on opposite sides of the NW (figure 4.14). By using just one Hall contact, the resolution requirements in the lithography process are relaxed and instead the etching of a spacer layer is used to control the contact overlap.

This geometry enables Hall effect in thinner nanowires than previously possible, simplifies the device fabrication significantly and makes Hall effect characterization available also in labs with somewhat less sophisticated fabrication tools. The downside of the three-probe device is that the measurement requires a relatively stable device where the resistance does not drift during the measurement. In a four-probe Hall device, such fluctuations will affect the potential in both contacts similarly and thereby cancel. If a three-probe Hall measurement is not carried out carefully, a drift in potential could be misinterpreted as a Hall voltage.

To monitor the drift and make sure that the signal is indeed a Hall voltage, the three-probe measurements can be carried out with a reference measurement taken at 0T between each step in magnetic field. In addition, the order of the magnetic field steps can be randomized. An example of such a measurement can be seen in figure 4.15a. By plotting the difference between the reference level and the measured potential
(this is the Hall voltage) versus the applied magnetic field, we can determine the Hall coefficient (figure 4.15b).

To extract the carrier concentration from the slope of the line in figure 4.15b, we need a model. Since the potential is only measured on one side of the nanowire, the Hall voltage measured in a three-probe geometry will be half that of one measured in a standard four-probe geometry. The three-probe Hall voltage in a cylinder can be written as

\[ V_{H,3p} = \frac{IB}{\pi nqr} \]  

(eq. 4.32)

where \( I \) is the current, \( B \) is the magnetic field, \( r \) is the radius of the nanowire and \( n \) is the carrier concentration. This kind of analytic expression is only valid if the contacts can be considered point-like, which in a nanowire device rarely is the case. To investigate how the contacts affect the measured Hall voltage, a three-probe Hall device was simulated using the FEM model previously described. Because the resistance of the contact metal is small compared to that of the semiconductor, the contacts were defined as iso-potential areas with a resistive boundary to the nanowire surface. This allows current to enter at one point of the contact and exit at another, providing a shunt path for the current passing through the device. This current shunting effect decreases the Hall voltage by reducing the current density right underneath the contact. Another deviation from the ideal analytic case is that the potential is not measured in a single point at the very top of the device, but instead in the area covered by the contact. This voltage shunting also reduces the Hall voltage.

The simulated deviation from the analytic model is presented in figure 4.16. First we study the case when the current shunting is limited by a large contact resistance (figure 4.16a). As expected, the Hall voltage decreases as the contact angle, defined as
the central angle of the circular sector that is covered with metal, is increased. It is worth noting that the Hall voltage is still present even when the contact angle is 180°. Next, we study the effect of contact resistance on the Hall voltage (figure 4.16b). Here we see that the Hall voltage decreases with decreasing contact resistivity, which is due to increasing shunting of current through the metal contact. Third (figure 4.16c), we find that nanowires with lower carrier concentration are more sensitive to current shunting due to the larger resistance in the nanowire compared to the contact shunt path. Finally (figure 4.16d), we observe that the current shunting effect is more prominent for thinner nanowires. In summary, the simulations show what is expected: the less point-like the contacts are, the larger deviation from the ideal case. The contacts should thus be designed to overlap the nanowire as little as possible and not be too wide. The deviations calculated here can be used as correction factors for Hall measurements on similar devices.

Figure 4.16. Simulated reduction in Hall voltage in three-probe Hall devices caused by non-point-like contacts. The Hall voltage is normalized with eq. 4.32. a) Normalized Hall voltage as function of contact angle. b) Normalized Hall voltage as function of contact resistivity for different contact angles angles. c) Normalized Hall voltage as function of contact resistivity for different nanowire carrier concentrations. d) Normalized Hall voltage as function of contact resistivity for different nanowire radii.
To test and verify this new kind of measurement, a series of InP nanowires was contacted in three-probe geometry. This series of nanowires was also studied using standard four-probe Hall measurements in paper III, allowing direct comparison of data measured with the two different techniques. The devices were fabricated using the same basic technique as described previously in this chapter. However, the etching of the spacer layer was done with a shorter time to give a smaller opening to the top of the nanowire. A sketch of the cross-section and an SEM image of a three-probe Hall device with two Hall contacts to enable two points of spatial resolution is shown in figure 4.17.

![a) Sketch of cross-section. b) SEM of device. Inset: Focused Ion Beam (FIB) cross-section. The scale bar is 100 nm.](image)

The contact angle, $\alpha$, was determined to be around 90° using top-view SEM and then verified by a FIB cross-section (inset in figure 4.17b). The contact resistivity of the devices was measured to be larger than $10^{-7} \Omega \text{cm}^2$. Using this for input in the correction factors calculated above, we can determine the charge carrier concentrations and compare them to four-probe Hall measurements (figure 4.18).
The comparison shows a good correlation between the four-probe and three-probe measurements, giving experimental verification that charge carrier concentration can be measured in three-probe geometry. Three-probe Hall measurements were also carried out on an InP nanowire with a diameter of only 65 nm. This is the thinnest nanowire with post-processed contacts characterized by Hall effect measurements so far, thus bridging the gap between nanowires thin enough to be fully depleted and characterized by field-effect measurements and nanowires with large enough diameter to be contacted for four-probe Hall effect measurements.
4.8 Hall effect measurements on GaN platelets

The platelet reformation process is done at conditions very different from standard epitaxy, making the properties difficult to predict. Thorough knowledge of the electrical properties is key to designing devices based on this technology. In order to measure carrier concentration, mobility and resistivity in a single platelet, a new Hall device was developed. The fabrication procedure was designed so that it can easily be adapted to platelet transistor fabrication. To fabricate a transistor, only minor changes to contact design and a few extra process steps would be necessary.

Platelets have a more compact shape than nanowires and cannot be broken off from the growth substrate as easily. Therefore, devices for characterization of single platelets are most easily fabricated directly on the growth substrate. There are two major challenges with this type of fabrication: First, when placing electrical contacts and large probe pads, care must be taken to electrically insulate the contact from everything but the selected platelet. The insulation must also be stable enough to withstand the physical force from the probes or bonding wires used to connect the device to the electronic test equipment. Second, the contacts must be placed with high accuracy both vertically and laterally, especially for devices with multiple contacts on a single platelet. The process described next uses a hydrogen silsesquioxane (HSQ) spacer layer instead of polymer to yield a device that can withstand higher contact annealing temperatures and has the potential to give low parasitic capacitance, for compatibility with high-frequency transistor applications.

4.8.1 Device fabrication for Hall characterization of platelets

First, a 50 nm thick Al₂O₃ film is deposited on the sample using atomic layer deposition to provide insulation and protect the semiconductor material from dry etch damage. Next, an approximately 400 nm thick layer of HSQ is spin coated and cured on the sample to cover the platelets and planarize the surface. A film of PMMA resist is then deposited and EBL is used to define a 2 µm wide hexagonal etch opening around the platelet to be contacted. The HSQ is then etched away from the top of the selected platelet using reactive ion etching (RIE). The RIE process etches HSQ, but not Al₂O₃, so the platelet is left with a protecting Al₂O₃ layer with a well-defined thickness that can be selectively wet etched using MF319. Finally, another layer of PMMA is deposited, contacts are defined using EBL and deposited using thermal evaporation. This fabrication process can easily be adapted for fabrication of various characterization devices, LEDs or transistors. A sketch and finished device for Hall characterization is shown in figure 4.19.
The geometry of the platelets makes the interpretation of the measured data challenging. The measured data was fitted to a FEM model to extract the resistivity and carrier concentration. By fitting the measured four-probe resistance (figure 4.20a) to the simulated potential distribution in the platelet (figure 4.20b), the resistivity was determined to be 4 mΩcm. Using the resistivity as an input parameter, the measured Hall voltage (figure 4.20c and 4.20d) could then be fitted to simulations and the carrier concentration and mobility was determined to be 5E18 cm$^{-3}$ and 300 cm$^2$/Vs respectively.
This carrier concentration is high for a nominally undoped semiconductor, and indicates that there are defects present. Since no dislocations are observed in transmission electron microscopy analysis, it is likely that the high conductivity is caused by point defects, most probably nitrogen vacancies. Tuning of reformation parameters to reduce the conductivity would make for an interesting future study. The high conductivity makes these platelets unsuitable for fabrication of junction-less transistors. However, for LEDs, high conductivity is not an issue.
5. Nanoscale optoelectronic devices

This chapter discusses the optoelectronic characterization presented in papers V-VI: An evaluation of Aerotaxy p-n junction nanowires intended for photovoltaic applications, and fabrication and characterization of nitride platelet LEDs.

5.1 Evaluation of Aerotaxy p-n junctions (paper V)

Aerotaxy is a synthesis technique which enables high-throughput production of high-quality nanowires in material systems suitable for photovoltaic applications. To build a solar cell it is necessary to construct a device able to separate charge, e.g. a p-n junction. In paper V we investigate the electro-optical properties of the first nanowires with p-n junctions synthesized by Aerotaxy. The Aerotaxy reactor used to grow these nanowires has multiple growth stages, enabling sequential growth of segments with different doping. A sketch of the reactor is shown in figure 5.1.

![Figure 5.1.](image)

Figure 5.1. Aerotaxy growth of nanowires with p-n junction. a) Generation of seed particles. b) Compaction of seed particles. c) Size-selection of seed particles. d) Alloying of seed particles with TMGa and DEZn. e) Growth of p-segment under supply of AsH₃. f) Further growth under supply of TMGa and AsH₃. g) Growth of n-segment under supply of TMGa, AsH₃ and TMSn. h) Collection of nanowires on a substrate.

This reactor is a development of the Aerotaxy system described in chapter 2. The main difference being the addition of dopants and the two extra growth chambers.
In order to assess the p-n junction nanowires, four-probe characterization devices were fabricated using the method previously described. A four-probe geometry was used to limit the effects of the contacts on the IV characteristic. The devices were evaluated using electrical measurements to study the characteristics of the p-n junction and the photo-response, by cathodoluminescence to study the doping profile, and finally by electron beam induced current (EBIC) measurements to determine the location of the p-n junction and the carrier diffusion length. The electrical measurements are presented in figure 5.2.

In dark conditions (figure 5.2a), the devices showed a strong rectifying behavior with an ideality factor of 1.9-2.0 and rectification ratio of more than $10^5$ at ±1 V. Note that the noise floor of the measurement setup is around $10^{-14} \, \text{A}$, setting a lower limit for the current measured at low voltages. Next, the nanowires were illuminated with a 532 nm diode laser to study the photo-response. The illuminated IV curves of device 1 from
figure 5.2a is presented in figure 5.2b. A clear photo-response with a short-circuit current increasing linearly with illumination intensity (figure 5.2c) and an open-circuit voltage of around 0.6 V, increasing with the logarithm of the illumination intensity (figure 5.2d). The $V_{OC}$ values are low compared to the band gap of GaAs (1.4 eV), but this is typical for unpassivated GaAs nanowires due to the large concentration of surface defects causing surface recombination and thus lowering $V_{OC}$. This is expected to improve significantly by implementing surface passivation, e.g. by growing a higher band-gap AlGaAs shell around the device. Surface recombination in the depletion region is also a likely explanation for both the shunt-resistance behavior seen in figure 5.2b and the ideality factor of 2.$^{140}$

The cathodoluminescence measurements clearly show shifts in the peak position of the spectrum, indicating charge carrier concentrations on the order of $10^{19}$ cm$^{-3}$. The EBIC measurements confirmed the presence of a well-defined p-n junction and showed that the minority carrier diffusion length is around 70 nm, similar to what has previously been measured for unpassivated GaAs nanowires grown by MOCVD.

This work shows that it is possible to synthesize high-quality nanowires with p-n junctions using the high-throughput Aerotaxy technique, an important step towards production of nanowire solar cells. It also demonstrates a toolbox of advanced characterization techniques that can be applied to the same single nanowire for a full evaluation of its properties. The ability to carry out thorough characterization on single nanowires is critical to get a fundamental understanding of the physics of nanowire-based devices and is key to improving the power conversion efficiency.
5.2 Nitride platelets for UV to red LEDs (paper VI)

The last paper to be discussed in this dissertation is about characterization of LEDs fabricated from nitride platelets. Three kinds of platelets are considered, InGaN platelets for green and red emission, GaN platelets for blue emission and GaN platelets with AlGaN layers for UV emission.

Fabricating LEDs from platelets is fundamentally different from fabrication of planar LEDs. Since the p-n junction in the platelet is exposed, it is necessary to cover the n-side before the top contact is deposited, otherwise the p-n junction would be short-circuited. Two fabrication schemes are outlined below. The first one for contacting multiple platelets in parallel to create an LED with large light output, and the second for contacting single platelets to make sub-micron LEDs for characterization and specialized research applications. By measuring on single platelets, it is possible to investigate variations between single platelets and not just the properties of an ensemble. The focus in this discussion is on device fabrication and characterization. Details on epitaxy will be published in separate papers by Khalilian and Bi.

5.2.1 Multiple platelet LEDs

The multiple platelet LED fabrication is done in five steps:

- 30 nm of aluminum oxide (Al₂O₃) is deposited using atomic layer deposition to protect the semiconductor material during the fabrication process and to provide electrical insulation (figure 5.3a).
- A polymer spacer layer (S1805) is spin coated on the sample, so the platelets are just barely covered (figure 5.3b). This resist layer can either be baked on a hot plate at 250 °C to make it permanent or at 120 °C to make it possible to remove.
- The spacer layer is thinned down in a RIE O₂ plasma process to remove the resist from the top facet of the platelets, so they can be accessed by the top contact (figure 5.3c).
- The Al₂O₃ covering the p-side of the platelets is etched away in a wet etch process (figure 5.3d).
- Metal is deposited to form a top contact (figure 5.3e). A shadow mask is used to define the contact area. A back contact can also be defined in this step by etching or mechanical removal or the resist, oxide and Si₃N₄ outside the platelet array before deposition of the metal.

This device fabrication could easily be adapted to using a more transparent spacer layer, e.g. HSQ or spin-on-glass. It is also be possible to remove the spacer layer before the metal deposition and rely on the insulation from the Al₂O₃ (as shown on the cover of
The fabrication process is compatible with a transparent oxide top contact (e.g. Indium tin oxide, ITO) or even a flip-chip device design. The simplicity of the design enables quick iterations and rapid electro-optical feedback for implementation of epitaxial improvements.

**Figure 5.3.** Fabrication of parallel platelet LED. a) Atomic layer deposition of Al₂O₃. b) Spin-coating of resist spacer. c) Etching of spacer layer. d) Etching of Al₂O₃. e) Deposition of top contact.

The main properties to characterize for parallel platelet LED devices is the IV characteristic and light output. If the top contact has a suitable size for accessing with an electrical probe (~200 µm in diameter), tens of thousands of platelets are contacted in parallel. Images of the light output of such devices is shown in figure 5.4b. Electroluminescence spectra for four different platelet LED devices emitting in UV, blue, green and red are shown in figure 5.4c. The spectra were acquired with a fiber spectrometer. The relatively narrow single-peak spectra indicate that the radiative
recombination takes place predominantly in the quantum wells and that the homogeneity between the platelets is good.

Since the IV characteristics are measured over a large ensemble of platelets, very high demands are placed on the homogeneity of the growth and precision of the fabrication. Figure 5.4d shows the IV characteristics of three different AlGaN comprising between 30 000 and 100 000 platelet LEDs in parallel. The rectification and diode behavior indicates that the homogeneity is indeed very good. An ideality factor larger than 2 is not surprising in a nitride LED due to the asymmetrically doped p-n junction and the difference in activation energy on the p and n side causing a weaker modulation of the recombination-limiting carrier density.\(^{103}\)

Figure 5.4. Characterization of multiplet platelet LEDs. a) Cross-section SEM of platelet LED device. b) Pictures of LEDs emitting in UV, blue, green and red. c) EL spectra of four platelet LED devices emitting in UV, blue, green and red. d) IV-characteristics of three multi-platelet LED devices.
5.2.2 Single platelet LEDs

Contacting single platelets is interesting both from a characterization viewpoint and for fabrication of extremely small light-emitters, e.g. for direct view displays with extremely high resolution. Just like in the process described in section 4.8, the main challenges of making contacts to single platelets on a chip is the spatial alignment of the contact and making sure the large bond pads are properly insulated from the platelets. The fabrication presented here is based on the multiple platelet design, but features a few extra steps. The fabrication is the same until the spacer layer has been etched down (figure 5.3c).

- After the first spacer layer has been etched down, another, thicker photoresist (S1813) is spin coated on the sample to act as a stable base for the bond pads. Using UV lithography, a 10 µm wide strip of resist is removed around the platelets that will be contacted. The lithography step is designed so that the spacer forms a smooth slope for the contact. The spacer is then baked at 250 °C to make it permanent. (Figure 5.5a).
- In an EBL process, ~1 µm openings are defined around the platelet to be contacted (figure 5.5b and 5.5c).
- The Al₂O₃ on the selected platelet is etched away in a wet etch process (figure 5.5d).
- Contacts are defined in a final EBL process and metal is deposited using thermal evaporation. Excess metal is removed in a lift-off process (figure 5.5e).
Figure 5.5. Fabrication of single platelet LED. a) Spin-coating and lithography definition of additional spacer to support the bond pads. b) Spin-coating of EBL resist. c) EBL exposure to open up for etching only selected platelets. d) Etching Al₂O₃. e) Deposition of top contact (defined by EBL).

Figure 5.6a is an optical micrograph showing seven blue-emitting single platelet LEDs. The additional contacts are open/short test structures. The measured IV-characteristics of single platelets (figure 5.6b) show excellent diode characteristics. Due to the small area of a single platelet and the noise floor of the measurement equipment (approx. 10 fA), it is not possible to resolve the reverse-current and parallel shunt resistance. However, the rectification is at least seven orders of magnitude. If the single platelet emission is bright enough, a spectrum can be recorded with the same method as for multi platelet LEDs (figure 5.6c, 5.6d). The full width at half maximum of the
spectrum is very similar to the multiple platelet blue LED spectrum shown in figure 5.4c (approx. 30 nm), indicating good homogeneity of the quantum wells throughout the platelet ensembles.

Figure 5.6. Single platelet devices. a) Optical micrograph showing seven single platelet LEDs. b) IV characteristics for five blue-emitting single platelet LEDs. c) Electroluminescence from a single platelet LED. d) Electroluminescence spectrum from a single platelet LED.

The fabrication and characterization of platelet LEDs presented here shows that platelets can function as high-quality sub-micron templates for growth of active layers. Much work lies ahead in increasing the efficiency, both by optimization of the device design and in improving the epitaxy. This realization of dislocation-free GaN and relaxed high In-composition InGaN pushes the boundaries of nitride epitaxy and opens up many new possibilities for high-performance optoelectronics as well as electronic devices.
6. Concluding remarks and outlook

Delving into the task of characterizing nanostructures has been a challenging and very interesting journey. Because of the many unknowns, it is always necessary to think thoroughly and question everything, from nanowire synthesis and surface properties to device fabrication, measurement methods, and not the least how to make sense of the measurements. Indeed, proper characterization at this scale is about assessing an entire system, not just taking a few measurements on a given device.

Doping characterization of nanostructures has matured significantly in the last five years and many elegant and interesting characterization techniques have been proposed by several different research groups. Much work has also been done to improve modeling for a more accurate extraction of material parameters from measurements. While no technique has emerged as a standard suitable for all kinds of nanowires, there are now several complementary electrical methods readily available to measure doping concentration in many nanoscale systems. I believe the work in this dissertation has contributed by developing new methods, improving models for analyzing measurements and by verifying the validity of existing methods. When it comes to nanoscale optoelectronics, the research community has evolved from proof-of-concept designs to impressive devices that have efficiencies comparable to their planar counterparts. I believe both Aerotaxy and nitride platelets are very interesting approaches for the next generation of optoelectronics and it has been very exciting to be part of these projects.

Perhaps the greatest challenge remaining for both doping characterization and optoelectronics at the nanoscale is to tame the surface properties. In devices where a poor surface dominates the device properties, meaningful characterization tends to be challenging and devices often perform poorly. The applicability of field-effect measurements is limited due to the capacitance reduction caused by interface traps and poor contacts make it hard to measure the relatively small Hall voltage. It would be very interesting to investigate further how the contact properties influence the Hall measurements, especially when it comes to Schottky contacts that very well can affect the carrier concentration in the nanowire significantly. The modeling framework is already in place, so the challenge would be to design a good experiment and find relevant input parameters. Furthermore, it would be very interesting to extract information about of surface defects from field-effect measurements and correlate it to another method, e.g. capacitance measurements. Another project that has been initiated, but has not progressed far enough to be included in this dissertation, is to
carry out nanowire Hall effect measurements at different temperatures to study doping activation energy, scattering mechanisms, etc.

For nanowire photovoltaics, controlling the surface recombination and the defects in the space charge region are key parameters to reach high efficiency. The same applies to LEDs. Some of this is epitaxy-related development, but important work also lies ahead in optimizing device design, contacts, passivation, spacers, etc.

To optimize the LED design, further studies are needed to measure and simulate the light outcoupling of the platelets and develop either a surface-emitting device with a good transparent contact or a flip-chip device with transparent substrate and a reflective contact. The extremely small platelet light emitters are also very interesting for use in direct-view displays with very high resolution and brightness. Extremely small LEDs can also be used in research applications. The use of single platelet LEDs for spatially resolved stimulation of cells for opto-genetic applications is currently being explored in a project that is outside the scope of this dissertation.

Furthermore, the nitride reformation process briefly discussed in this dissertation has many very interesting applications. Dislocations are not only affecting the performance of optoelectronics, but also very much the performance of power electronics. In particular, dislocations are detrimental to the breakdown voltage of GaN devices, thereby limiting the use of GaN in high-voltage devices. Much exciting work lies ahead in exploring the full potential of reformed dislocation-free GaN in electronics.
The research presented in this dissertation would not have been possible without the outstanding collaborations and brilliant colleagues I have had during these five years. The excellent fabrication facilities and cutting-edge epitaxy in combination with the open and collaborative environment really makes the Nano Lund environment a great place to do nanoscience.

To my advisors:
Lars Samuelson, thank you for giving me the opportunity to do research in this great environment, for your support, inspiration, enthusiasm and confidence in me. You have always showered me with excellent and innovative ideas for research, but also given me great freedom to try my own ideas.

Kristian Storm, thank you for everything that you have taught me, for your positive energy, believing in me, always being available to help or discuss and always giving me a push in the right direction when I needed it. I appreciate that it is straightforward and easy to discuss things with you.

Magnus Borgström, thank you for always having your door open, being helpful and looking out for me. Your honesty is always refreshing!

Mikael Björk, thank you for giving me the opportunity to collaborate with Sol Voltaics and for your support and encouragement.

Thanks to all my other colleagues. It has been so much fun to work with all of you. Special thanks to the ones that I have worked and collaborated with more closely, I have learned very much from you:
Gaute Otnes, Magnus Heurlin, Maryam Khalilian, Rafal Ciechonski, Zhaoxia Bi, Taiping Lu – thanks for all the excellent epitaxy work and discussions.
Martin Berg, Karl-Magnus Persson, Fredrik Lindelöw, Renato Mourão, Ali Nowzari and Lukas Wendt – thanks for all the inspiration, ideas and great collaborations in the lab.
David Lindgren, Enrique Barrigón, Linda Johansson, Vilgailė Dagytė, Jovana Colvin, Pyry Kivisaari, Bo Monemar and Anders Gustafsson – thanks for all the interesting discussions and collaborations.
Jonas Ohlsson, you have been like an extra advisor for me. Thank you for always making time for me.

To my office mates: Alexander, Bekmurat, Fangfang and Yuwei, thanks for the company!
Thanks to the lab staff for all help with the equipment and your positive attitude. You make Lund Nano Lab a great place to work.

Niklas, our friendship has been so important to me during these years. You always make sure I keep my head high and make me feel like nothing is too difficult.

Eva, Torleif and Erik, thank you for always believing in me, for all your support and encouragement. Thanks also to my extended family for all your care and support.

Last, but certainly not least, Ylva. Thank you for always being there with love, joy, care, support and encouragement. You are my sunshine.
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Nanostructures for Optoelectronics
Device Fabrication and Characterization

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