1/f-noise in Vertical InAs Nanowire Transistors

Persson, Karl-Magnus; Berg, Martin; Lind, Erik; Wernersson, Lars-Erik

Published in:
2013 International Conference on Indium Phosphide and Related Materials (IPRM)

DOI:
10.1109/ICIPRM.2013.6562634

2013

Link to publication

Citation for published version (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
1/f-noise in Vertical InAs Nanowire Transistors

Karl-Magnus Persson, Martin Berg, Erik Lind, and Lars-Erik Wernersson
Department of Electrical- and Information Technology
Lund University
Lund, Sweden
karl-magnus.persson@eit.lth.se

Abstract—The material quality at high-κ interfaces are a major concern for FET devices. We study the effect on two types of InAs nanowire (NW) transistors and compare their characteristics. It is found that by introducing an inner layer of Al₂O₃ at the high-κ interface, the low frequency noise (LFN) performance regarding gate voltage noise spectral density, Sᵥᵥ, is improved by one order of magnitude per unit gate area.

Keywords—1/f-noise; high-κ; nanowire; InAs; FET

I. INTRODUCTION

InAs nanowire (NW) FETs are a good candidate for future RF electronics, promising both low power dissipation and high speed operation [1][2][3]. To verify the feasibility in the technology, however, it is vital to fabricate high performance devices. By utilizing different evaluation methods, the delicate balance of different processing conditions can be evaluated; for a FET, good control over the interfaces is essential. Besides measurements of the I-V characteristics, it is of interest to determine the trap density and one common method is measurement of low frequency noise (LFN). In this abstract, we investigate the differences in LFN as well as Iₒᵣ, Sᵢᵣ, DIBL, and other metrics for devices fabricated with two different high-κ films, HfO₂ and Al₂O₃/HfO₂, implemented for DC and RF operation, respectively [4][5].

II. FABRICATION

A. DC Devices

InAs NWs are grown on a doped InAs substrate. Seed Au particles defined with electron beam lithography (EBL) determines diameter, here 40 nm, and placement. The growth is made in a metal-organic-vapor-phase-epitaxy (MOVPE) growth chamber at 420 °C and with a Sn dopant molar fraction of 3.49·10⁻⁸. The high-κ film is deposited both before and after the fabrication of the first separation layer. The two high-κ films, consisting of HfO₂, is deposited with atomic layer deposition (ALD) at 250 °C and is in total 7 nm, with an EOT of 1.5 nm. The source-gate separation layer consists of a 30 nm evaporated SiOₓ film. During evaporation, the sample is tilted so that there will be a buildup of flakes on sides of the NWs, which can be removed in a wet-etch, leaving the lateral layer intact. This process is also used for the evaporated Ni gate and the film thickness sets Lₒ = 35 nm (Fig. 1a). The evaporated top metal is elevated with a spin-on polymer resist which is back etched.

B. RF Devices

To accommodate RF transistors and circuits, the DC device structure was refined; devices are placed on an isolating substrate. Also, targeting high yield, the gate process is exchanged. The processing flow chain begins with growth of a 300-nm-thick InAs layer on top of a Si substrate to mitigate growth of InAs NWs, and also, to act as contact mesa structure after being etched out. NWs with a diameter of 45 nm are grown at 420 °C and with a Sn dopant molar fraction of 1.07·10⁻⁷. For both devices, the NWs are homogenously doped. The high-κ film is deposited with ALD and consists of 0.5 nm Al₂O₃ at 250 °C and 6.5 nm of HfO₂ at 100 °C, with a total EOT of 1.8 nm. The W-gate is sputtered with a layer thickness of 60 nm and is separated from the source mesa with a 60 nm Si₃N₄ film deposited with plasma enhanced chemical vapor deposition (PECVD) in a preceding step. The nitride film is removed from the sides of the NWs with a dry etch. The gate length is set by a defining polymer and a dry etch, giving Lₒ ≥ 200 nm (Fig. 1b). The top metal is sputtered and is elevated by a spin-on polymer resist that is back etched.

III. MEASUREMENT AND RESULTS

Devices are measured with a Keithley 4200 SCS and for the LFN characterization, a Lock-in amplifier and a LNA are added to the setup. The 1/f-noise is measured for Vₒᵣ = 50 mV and f = 10 Hz. Obtained data from measurements of normalized current noise spectral density, Sᵢᵣ/Iₒᵣ², is shown in

---

This work has been supported by the Swedish Foundation for Strategic Research and VINNOVA.
Fig. 2. Two curves have been added, $g_m/\mu_{DS}$ and $1/I_{DS}$, where the shape of the curves are indicative for LFN dominated by number fluctuations and mobility fluctuations, respectively. The factor of $30k$ was multiplied curves are indicative for LFN dominated by number fluctuations and $2/\mu_{DS}$ for the two different high-k devices, the improvement is one order of magnitude for $S_{Vg}$ and about two orders of magnitude for $S_{\mu}/I_{DS}^2$. As the numbers given for the $S_{Vg}$ are normalized to the gate area, the difference in the amount of charges for different channel lengths is accounted for. The data suggest that there is a lower interface trap concentration with the introduction of an Al,O$_3$ film and the improvement can possibly be traced to a reduction in sub-oxides [6]. The reason for the SS degradation could be explained by the increase in doping and the inability to deplete the channel all the way through. This is partly the explanation for the increase in DIBL as well, where the undepleted carriers form a parallel parasitic resistance. The DIBL is also likely to be caused by other effects such as band-to-band tunneling. To accommodate the issue concerning the channel depletion, the wire diameter, $D_{NW}$, should be scaled and it has been shown that scaling the diameter to 28 nm improves the off characteristics (SS = 80/140 mV/V for $V_{DS} = 0.05/0.5$ V) keeping other parameters constant (although EOT = 1.3 nm) [5]. To maintain good on-performance when scaling, however, it is necessary to address the increase in series resistance; this could be done by, for example, introducing a heterogenous doping profile and/or thinning down the separation layers [3].

**ACKNOWLEDGMENT**

The authors would like to thank Mattias Borg, Jun Wu, and Johannes Svensson for growth of nanowires and materials.

**REFERENCES**


